1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J113 MLB SCHEMATIC
10/03/14

3_1_PP3V42_G3H给U1900供电后输出PPVRTC_G3H和PCH_CLK32K_RTCX1
3_2_PPVRTC_G3H给PCH提供VCCRTC供电和RTCRST#、SRTCRST#复位
3_3_PPVRTC_G3H给PCH的INTVRME供电，开启PCH内部1.05v浅睡眠待机供电
3_4_PPVRTC_G3H给PCH的DSWVRMEN供电，开启PCH内部1.05v深度睡眠待机供电
3_5_PCH_CLK32K_RTCX1给PCH提供RTC时钟
3_6_EC得到SMC_BC_ACOK后，自动发出SMC_PM_G2_EN,送给U7501第12脚EN,用于开启待机芯片的线性电压;SMC_PM_G2_EN改名S5_PWR_EN又改名P3V3S5_EN_R,送给U7501
3_7_U7501得到PPBUS_G3H转过来的VIN、EN后输出线性电压;得到EN2后，控制第二路PWM输出PP3V3S5
3_8_当PP3V3_S5正常后，U7501开漏输出S5_PWRGD.
3_9_PP3V3_S5给PCH的深度睡眠待机VCCDSW3_3供电
3_10_U7501开漏输出的S5_PWRGD经PP3V42_G3H上拉送给EC,EC发出PM_DSW_PWRGD给PCH的DPWROK
3_11_PCH得到VCCDSW3V2和DPWROK后发出PM_SLP_SUS_L
3_12_PM_SLP_SUS_L改名为P3V3SUS_EN后送给U8020把PP3V3_S5转化为PP3V3_SUS
3_13_PP3V3_SUS，给PCH的VCCSUS3、VCCSPI供电；给BIOS的U6100供电；给U7840后产生PP1V05_SUS线性电压；给U8130的SENSE脚，用于检测PP3V3_SUS的电压。
3_14_U8130检测到SENSE的电压高于3.07V后，开漏输出RESET*,经上拉产生RSMRST_L送给PCH的RSMRST#
3_15_EC检测到适配器电压、电池电压，EC会发出SMC_ADAPTER_EN给PCH的ACPRSENT;EC还会发出PM_BATLOW_L给PCH的BATLOW*
3_16_PCH收到以上信号后，发出PCH_SUSWARN_L和PM_CLK32K_SUSCLK_R给EC。

1_1_PPDCIN_G3H经Q7010自导通产生PPDCIN_G3H_ISOL
1_2_PPDCIN_G3H_ISOL给ISL6299供电和开启及U7090供电和开启产生PP3V42_G3H
1_3_PP3V42_G3H给ISL6259提供复位SMB_RESET_N
1_4_ISL6259的第6脚CELL接地，设置电芯串联数量为2
1_5_以上条件满足后ISL6259开启Q7180并控制产生PPBUS_G3H;开漏输出SMC_BC_ACOK给EC作适配器检测

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5_1_PM_SLP_S5_L后一路进入EC，一路改名S4_PWR_EN
5_2_PM_SLP_S4_L与S4_PWR_EN，共同产生USB_PWR_EN,去开启S5、S4下的USB供电;共同产生P5VS4RS3_EN去开启5VPWM供电PP5V_S4RS3;
5_3_PM_SLP_S4_L分别改名P3V3S3_EN、P1V8S3_EN、DDRREG_EN
5_4_P5VS4RS3_EN送给U7501的EN1，开启PP5VS4RS3,正常后，U7501延时产生PGOOD1输出，改名为P5VS4RS3_PGOOD
5_5_P3V3S3_EN送给U8010开启PP3V3_S3,P1V8S3_EN送给U7820,开启PP1V8_S3,并输出P1V8S3_PGOOD;DDRREG_EN送给U7400,开启内存主供电PP1V2_S3,并输出DDRREG_PGOOD
5_6_PM_SLP_S3改名PM_SLP_S3_BUF_L、P5VSO_EN、P3V3SO_EN、P1VO5SO_EN。分别送往各自的芯片开始供电。
5_7_以上所有供电正常后，各路PG相与产生ALL_SYS_PWRGD，ALL_SYS_PWRGD送往EC,EC再延时输出SMC_DELAYED_PWRGD。ALL_SYS_PWRGD送给U1930与PM_SLP_S3_L相与，开漏输出CPU_VCCST_PWRGD。
5_8_CPU_VCCST_PWRGD直接送给CPU的VCCST_PWRGD脚，后CPU发出SM_PG_CNT1和VR_EN两信号，分别去开启CPU核心供电和内存VTT电压。
5_9_ALL_SYS_PWRGD送往并产生PM_PCH_SYS_PWROK，PM_PCH_PWROK
5_10_PM_PCH_SYS_PWROK，PM_PCH_PWROK送往CPU的SYS_PWROK、PCH_PWROK、APWROK。
5_11_CPU供电正常后，晶振起振，然后通过SPI总线读取BIOS信息配置CPU的GPIO脚位
5_12_CPU发出PROCPWRGD,CPU延时发出PLTRST#，然后发出SVID重新调整CPU供电。
5_12_CPU工作条件满足后，读取BIOS程序，开始自检，当检查完显卡后亮机。

2_1_PP3V42_G3H给EC待机供电，后12M晶振起振给EC提供时钟
2_2_P3V42_G3H给U5110供电，后发出PP3V3_s5_AVREF_SMC给EC的VREFA+脚供电。同时发出SMC_RESET_L给EC做待机复位。
2_3_在插入适配器瞬间，EC得到供电、时钟、复位、程序、SMC_BC_ACOK后通过SYS_ONEWIRE总线读取适配器信息，绿灯亮起。

4_1_按下键盘上的开机键，产生SMC_ONOFF_L给EC,EC发出PM_PWRBTN_L给PCH，PCH待机正常及收到PWRBTN#后，发出PM_SLP_S%_L、PM_SLP_S4_L、PM_SLP_S3_L和PM_SLP_S0_L

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051 00385	1	SCHEM MLB J43A	SCH	CRITICAL	
820 00165	1	PCBF MLB J43	PCB	CRITICAL	

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING
TITLE MLB
ABBREV DRAWING
LAST_MODIFIED Fri Oct 3 11 36 00 2014

DRAWING TITLE: <PART_DESCRIPTION>
Apple Inc.
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:PVT,MLB_PROGPARTS
MLB_MISC	PP5V5 DCIN NO TBTHV P15V EDP CAM XTAL NO CAM WAKE NO APCLKRQ ISOL TPAD INTWAKE SHARED USB PWR S3 SD ON MLB VCORE FETS SSD LPSR S3
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	XDP,SAMCONN
MLB_DEBUG:PVT	BKLT:PROD,XDP,SAMCONN,ISNS:ENG,DBGLED,XDP_CONN
MLB_DEBUG:PROD	BKLT:PROD,SAMCONN,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU H5 ISNS:YES CPUVR ISNS:YES DRAM ISNS:YES P5V0S ISNS:YES AIRPORT ISNS:YES SSD ISNS:YES LCDBKLT ISNS:YES P3V3S ISNS:YES 3V3S0 ISNS:YES OTHER H5 ISNS:YES CAM ISNS:YES CPU0DR ISNS:YES PANEL ISNS:YES
ISNS:PROD	CPU H5 ISNS:YES CPUVR ISNS:YES DRAM ISNS:YES P5V0S ISNS:NO AIRPORT ISNS:NO SSD ISNS:YES LCDBKLT ISNS:NO P3V3S ISNS:NO 3V3S0 ISNS:NO OTHER H5 ISNS:NO CAM ISNS:NO CPU0DR ISNS:NO PANEL ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:MICRON_8GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:MICRON_8GB
DDR3:HYNIX_16GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_16GB
DDR3:SAMSUNG_16GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:SAMSUNG_16GB
DDR3:ELPIDA_16GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_16GB
DDR3:MICRON_16GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:MICRON_16GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0915	1	EEPROM 4MBIT SPI 50MHZ 1 8V USON8	U2890	CRITICAL	TBTROM:BLANK
341S00159	1	T29 EEPROM FALCON RIDGE(V27 1) PROto 0 J110/J113	U2890	CRITICAL	TBTROM:PROG
338S1214	1	IC SMC12 B1 40MHZ/56OMIPS MCU 157BGA	U5000	CRITICAL	SMC:BLANK
335S00006	1	IC SERIAL FLASH 64 MBIT 3V WSON QE 1	U6100	CRITICAL	BOOTROM MAC BLANK
335S00007	1	IC SERIAL FLASH 64 MBIT 3V WSON QE 1	U6100	CRITICAL	BOOTROM NUM BLANK
341S00153	1	IC EFI ROM(V0108)) PROTO 0 J110/J113	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00029	1	BDW QGH9 D0 1 8 15W 2+2 0 7 4M B1168	U0500	CRITICAL	CPU:2.1GHZ
337S00073	1	BDW QGHB D0 1 6 15W 2+2 0 6 4M B1168	U0500	CRITICAL	CPU:1.6GHZ
338S00069	1	IC TBT FR 2C 288 12x12 FC CSP TRAY	U2800	CRITICAL	
338S1264	1	IC BCM15700A2KFEB4G S2 CMRA 8XB 208FCBGA	U3900	CRITICAL	
607-6811	1	ASSEMBLY SUBASSY PCBA HALL EFFECT K99	J6955	CRITICAL	J113_MLB
946-5477	1	UV GLUE MLB J41 J43	GLUE	CRITICAL	
825-7987	1	LABEL,MLB,J41/J43	NEW_LABEL		
376S00036	2	MOSFET N CH 30V 52A 5 9M 8P 3 3X3 3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S00037	2	MOSFET N CH 30V 64A 3 5M 8P 3 3X3 3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1194	2	MOSFET N CH 30V 15 3A 12M 8P 3 3X3 3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET N CH 30V 22A 6 0M 8P 3 3X3 3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE HYNIX 4GB
333S0681	4	IC SDRAM 16Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE HYNIX 8GB
333S00001	4	IC SDRAM 23NM 8GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE SAMSUNG 4GB
333S00003	4	IC SDRAM 23NM 16GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE SAMSUNG 8GB
333S0793	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 4GB
333S0791	4	IC SDRAM 16Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 8GB
333S0793	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE MICRON 4GB
333S0791	4	IC SDRAM 16GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE MICRON 8GB
333S0789	4	IC SDRAM 25nm 32Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 16GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
4GB	0	0
8GB	0	1
16GB	1	0
RSVD	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Vale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	20Mhz Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S00014	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
870-5074	870-1938		ALL	ALT POGO PIN W O CAP
860-3428	860-1327		ALL	ALT STANDOFF W O MYLAR
333S0787	333S0677	DRAM TYPE HYNIX 4GB	ALL	ALT STANDOFF W O MYLAR
860-3690	860-1328		ALL	ALT STANDOFF W O MYLAR
333S0785	333S0681	DRAM TYPE HYNIX 8GB	ALL	ALT STANDOFF W O MYLAR
353S3814	353S3812		ALL	ALT TBT PORT MUX
311S00008	311S0271		ALL	ALT AND GATE
311S00007	311S0426		ALL	ALT SNGL BUFFER
311S00015	311S0450		ALL	ALT 2-INPT AND
311S00013	311S0508		ALL	ALT SNGL BUFFER
311S00014	311S0515		ALL	ALT DUAL BUFFER
353S00133	353S2741		ALL	ALT PWR DIST SW

SYNC MASTER=J43_MLB SYNC_DATE=01/17/2013

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BOM Configuration

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00623	PCBA,MLB,BEST,HY-4GB,X430	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00624	PCBA,MLB,BEST,HY-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00625	PCBA,MLB,BEST,HY-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_16GB
639-00626	PCBA,MLB,BEST,SM-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00627	PCBA,MLB,BEST,SM-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00628	PCBA,MLB,BEST,MI-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_4GB
639-00629	PCBA,MLB,BEST,MI-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_8GB
639-00630	PCBA,MLB,BEST,MI-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_16GB
639-00631	PCBA,MLB,BEST,EL-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_4GB
639-00632	PCBA,MLB,BEST,EL-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_8GB
639-00633	PCBA,MLB,BETTER,HY-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00634	PCBA,MLB,BETTER,HY-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00635	PCBA,MLB,BETTER,HY-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_16GB
639-00636	PCBA,MLB,BETTER,SM-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00637	PCBA,MLB,BETTER,SM-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00638	PCBA,MLB,BETTER,MI-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_4GB
639-00639	PCBA,MLB,BETTER,MI-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_8GB
639-00640	PCBA,MLB,BETTER,MI-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_16GB
639-00641	PCBA,MLB,BETTER,EL-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB
639-00642	PCBA,MLB,BETTER,EL-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB
685-00046	CMN PTS,PCBA,MLB,X433	MLB_COMMON,J113_MLB
685-00047	VCORE FET,REN,X433	VCORE_FET:REN
685-00048	VCORE FET,VSHY,X433	VCORE_FET:VSHY
639-00697	PCBA,MLB,BETTER,EL-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00047	685-00048		ALL	Renesas alt to Vishay

333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1246	1	IC GL3219 USB3 SD CARD READER 46P LQFN	U4500	CRITICAL	

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00148	1	IC SMC B1 EXT(Vxxxx) PROTO 0 J113	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00046	1	CMN PTS,PCBA,MLB,J113	CMNPTS	CRITICAL	MLB_CMNPTS
685-00048	1	VCORE FET,VSHY,J113	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN TOPSIDE ALT J41/J43	TBTTOPSIDE 2P FENCE	CRITICAL	
806-5108	1	CAN TOPSIDE COVER ALT J41/J43	TBTTOPSIDE 2P COVER	CRITICAL	
806-3142	1	CAN TBT J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN COVER TBT J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN MDP J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD USB MLB J11/J13	USBCAN	CRITICAL	

Plated Board Slot

SL0400
TH-NSP
SL 2 3X3 9 2 9X4 5

CPU Heat Sink Mounting Bosses

Z0413
STDOFF-4.5OD1.52H-SM

Z0410
STDOFF-4.5OD1.52H-SM

Z0411
STDOFF-4.5OD1.52H-SM

Z0412
STDOFF-4.5OD1.52H-SM

4x 860-1327

Fan Boss

Z0405
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0414
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0415
STDOFF-4.5OD1.9H-SM
860-1327

Can Slots

SL0401
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0402
TH-NSP
SL-1.1X0.4-1.4X0.7

2x TBT pin diodes

SL0403
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0406
TH-NSP
SL-1.1X0.4-1.4X0.7

2x MDP Connector

SL0405
TH-NSP
SL 1.1X0.45-1.4X0.75

SL0407
TH-NSP
SL-1.1X0.45-1.4X0.75

2x TBT chip

SL0404
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0408
TH-NSP
SL-1.1X0.4-1.4X0.7

2x USB Connector

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0405
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0406
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
PD PARTS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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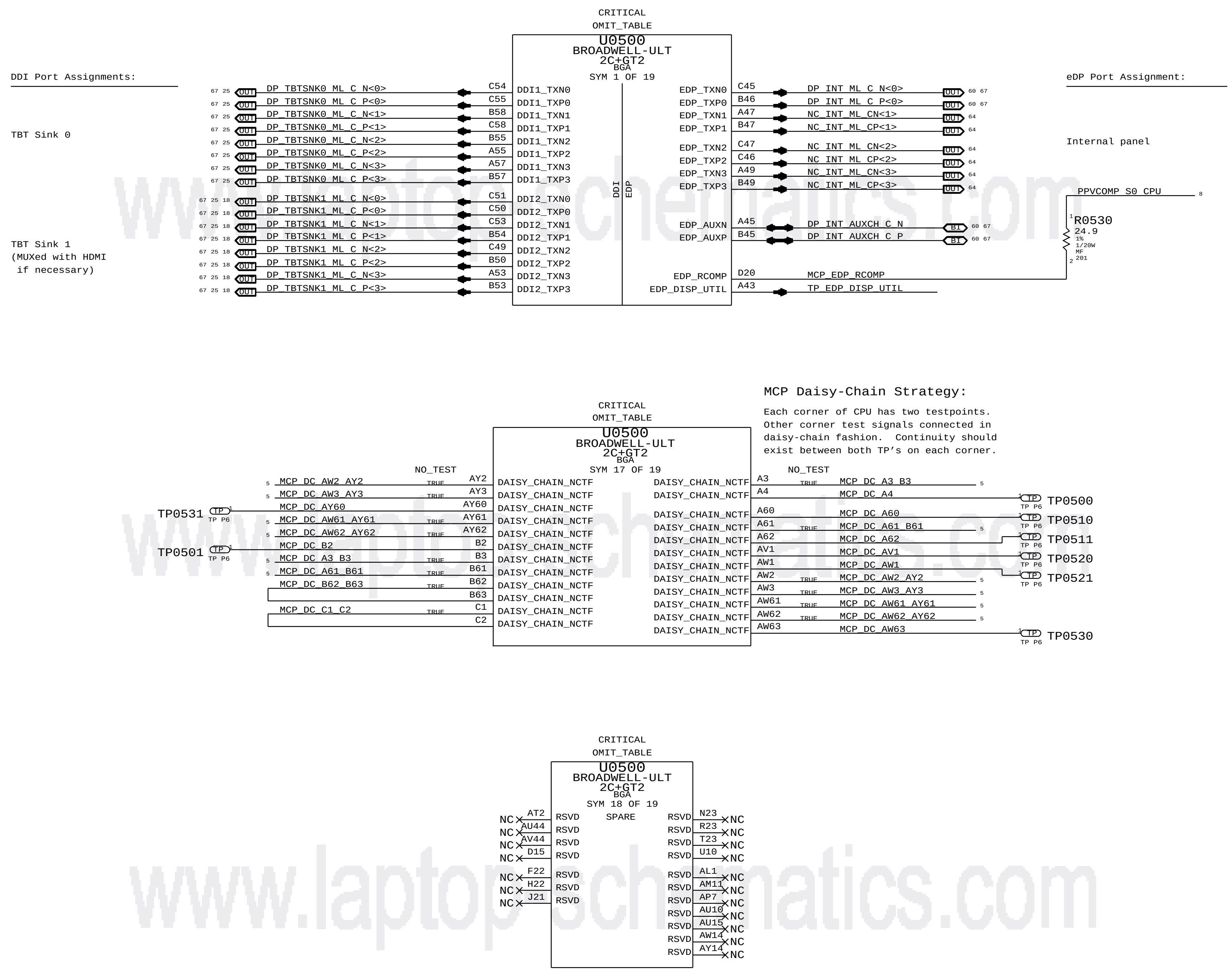


CPU GFX/NCTF/RSVD

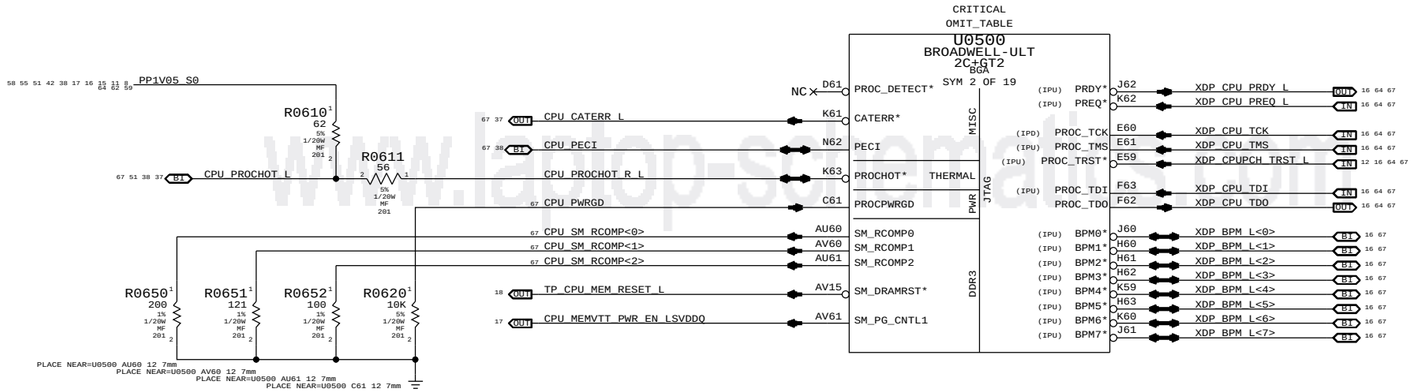
SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

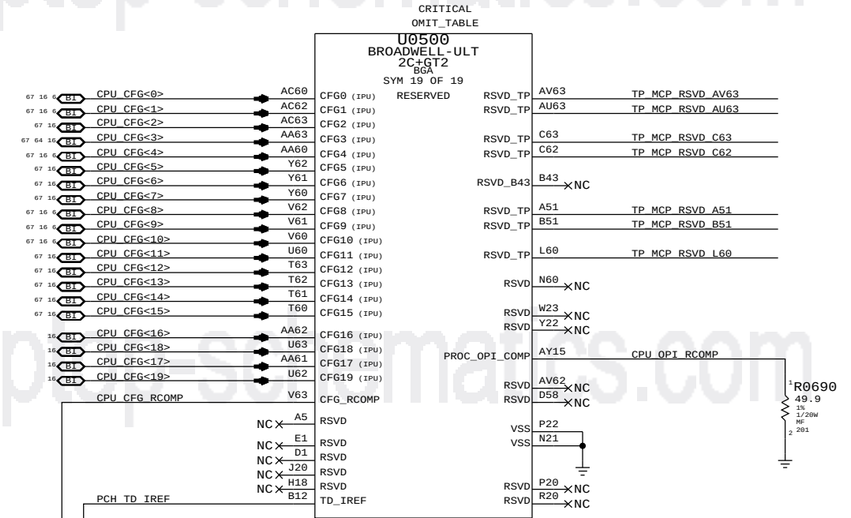
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

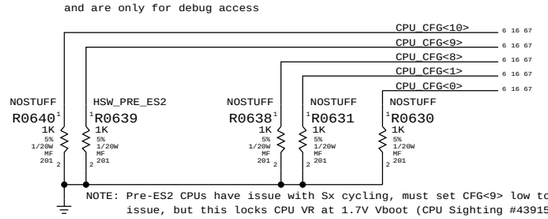
BRANCH <BRANCH>



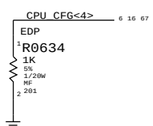


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC MASTER=WILL_J43	SYNC DATE=09/13/2012
PAGE TITLE	CPU Misc/JTAG/CFG/RSVD
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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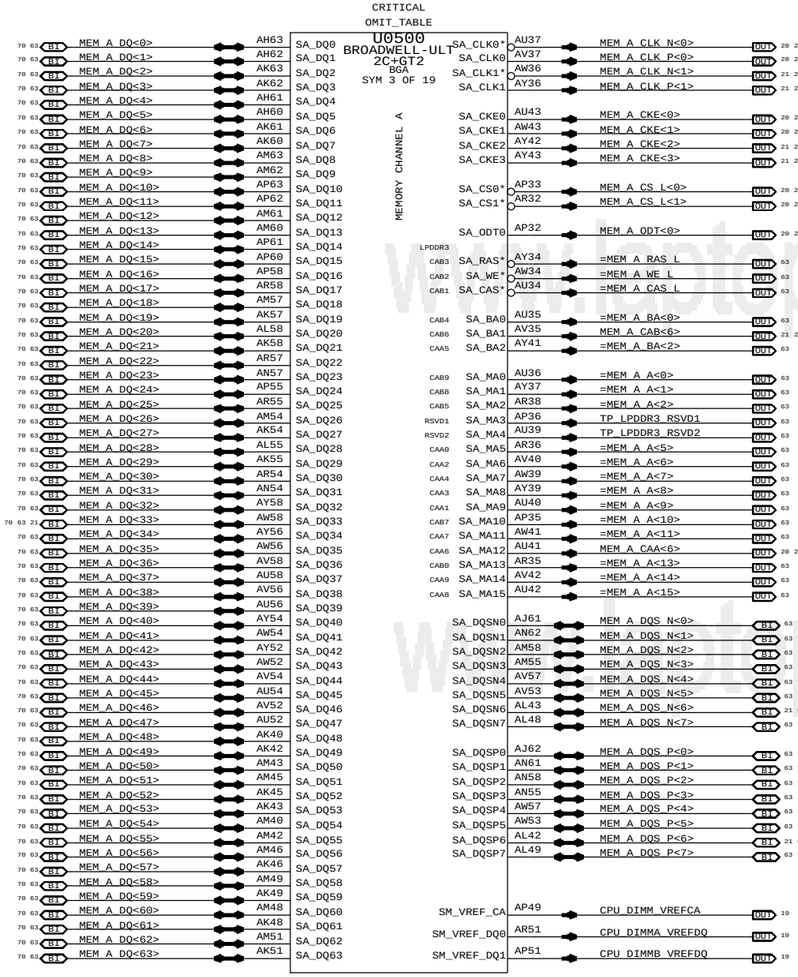

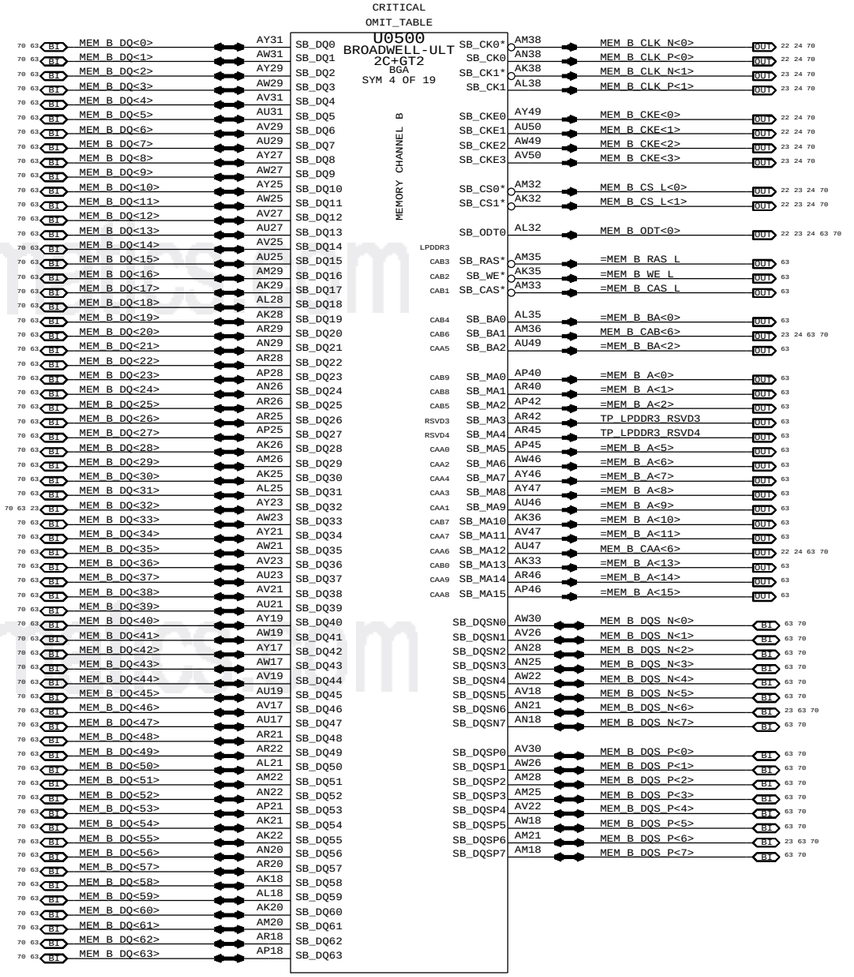

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PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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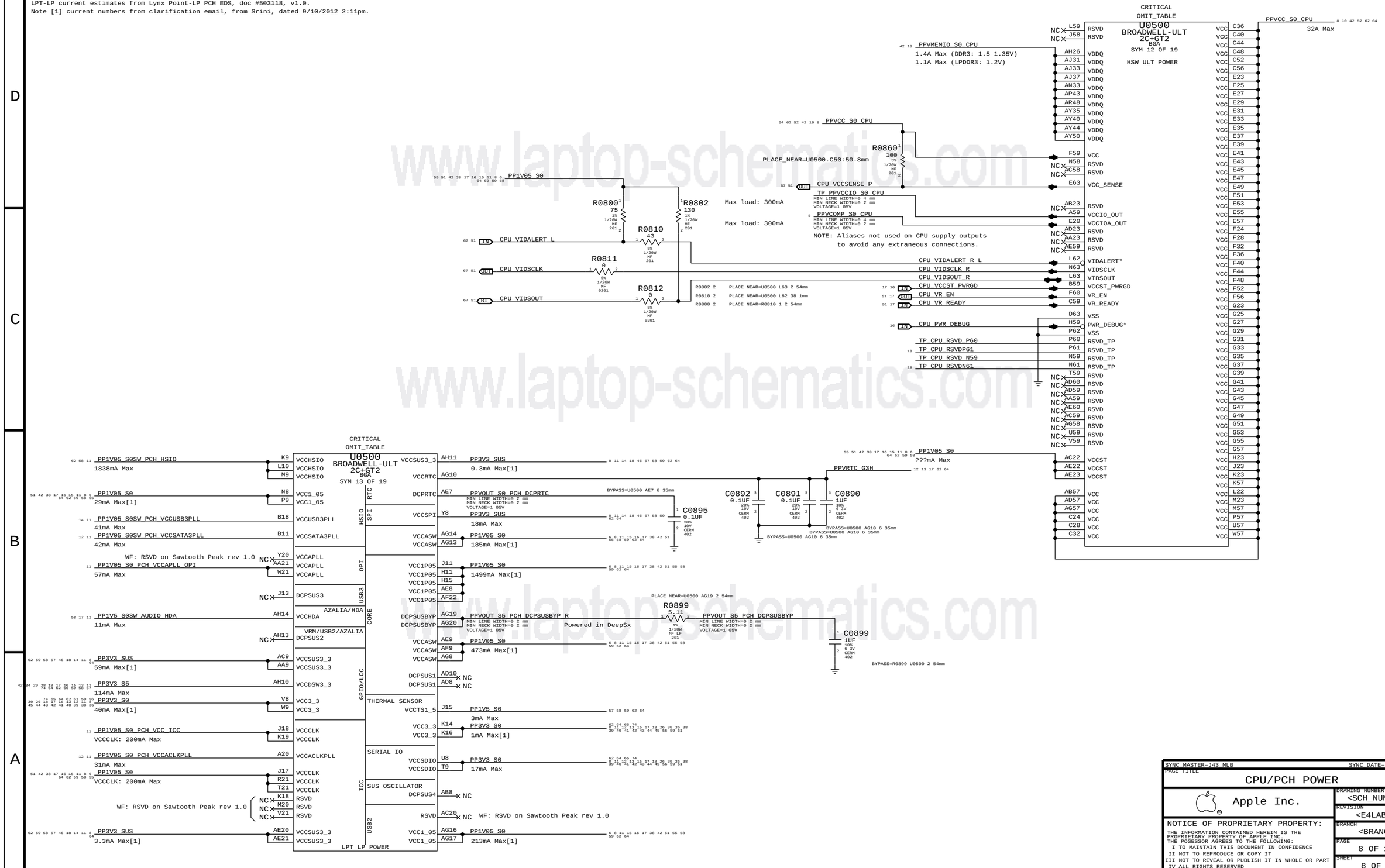
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE: CPU/PCH POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
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AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N → OUT 51 67

R0960
100
5% 1/20W MF 201
1 2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1 0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

64 62 52 42 8 PPVCC_S0_CPU

CRITICAL C1000 10UF 20% 4V X6S 0402	CRITICAL C1001 10UF 20% 4V X6S 0402	CRITICAL C1002 10UF 20% 4V X6S 0402	NO STUFF C1003 10UF 20% 4V X6S 0402	CRITICAL C1004 10UF 20% 4V X6S 0402	NO STUFF C1005 10UF 20% 4V X6S 0402	NO STUFF C1006 10UF 20% 4V X6S 0402	CRITICAL C1007 10UF 20% 4V X6S 0402	NO STUFF C1008 10UF 20% 4V X6S 0402	NO STUFF C1009 10UF 20% 4V X6S 0402	CRITICAL C1010 10UF 20% 4V X6S 0402	NO STUFF C1011 10UF 20% 4V X6S 0402	CRITICAL C1012 10UF 20% 4V X6S 0402	NO STUFF C1013 10UF 20% 4V X6S 0402	CRITICAL C1014 10UF 20% 4V X6S 0402	NO STUFF C105A 10UF 20% 4V X6S 0402	NO STUFF C105B 10UF 20% 4V X6S 0402	NO STUFF C105C 10UF 20% 4V X6S 0402	NO STUFF C105D 10UF 20% 4V X6S 0402	NO STUFF C105E 10UF 20% 4V X6S 0402	NO STUFF C105F 10UF 20% 4V X6S 0402
NO STUFF C1015 10UF 20% 4V X6S 0402	CRITICAL C1016 10UF 20% 4V X6S 0402	CRITICAL C1017 10UF 20% 4V X6S 0402	CRITICAL C1018 10UF 20% 4V X6S 0402	NO STUFF C1019 10UF 20% 4V X6S 0402	NO STUFF C1020 10UF 20% 4V X6S 0402	CRITICAL C1021 10UF 20% 4V X6S 0402	NO STUFF C1030 10UF 20% 4V X6S 0402	NO STUFF C104A 10UF 20% 4V X6S 0402	NO STUFF C104B 10UF 20% 4V X6S 0402	NO STUFF C104C 10UF 20% 4V X6S 0402	NO STUFF C104D 10UF 20% 4V X6S 0402	NO STUFF C104E 10UF 20% 4V X6S 0402	NO STUFF C104F 10UF 20% 4V X6S 0402	NO STUFF C106A 10UF 20% 4V X6S 0402	NO STUFF C106B 10UF 20% 4V X6S 0402	NO STUFF C106C 10UF 20% 4V X6S 0402	NO STUFF C106D 10UF 20% 4V X6S 0402	NO STUFF C106E 10UF 20% 4V X6S 0402		
NO STUFF C1070 10UF 20% 4V X6S 0402	NO STUFF C1071 10UF 20% 4V X6S 0402	NO STUFF C1072 10UF 20% 4V X6S 0402	NO STUFF C1073 10UF 20% 4V X6S 0402	NO STUFF C1074 10UF 20% 4V X6S 0402	NO STUFF C1075 10UF 20% 4V X6S 0402	CRITICAL C1076 10UF 20% 4V X6S 0402	CRITICAL C1077 10UF 20% 4V X6S 0402	NO STUFF C1078 10UF 20% 4V X6S 0402	NO STUFF C1079 10UF 20% 4V X6S 0402	NO STUFF C1080 10UF 20% 4V X6S 0402	NO STUFF C1081 10UF 20% 4V X6S 0402	NO STUFF C1082 10UF 20% 4V X6S 0402	CRITICAL C1083 10UF 20% 4V X6S 0402	CRITICAL C1084 10UF 20% 4V X6S 0402						
NO STUFF C1085 10UF 20% 4V X6S 0402	NO STUFF C1086 10UF 20% 4V X6S 0402	NO STUFF C1087 10UF 20% 4V X6S 0402	CRITICAL C1088 10UF 20% 4V X6S 0402	CRITICAL C1089 10UF 20% 4V X6S 0402	NO STUFF C1090 10UF 20% 4V X6S 0402	NO STUFF C1091 10UF 20% 4V X6S 0402	NO STUFF C1092 10UF 20% 4V X6S 0402	NO STUFF C1093 10UF 20% 4V X6S 0402	NO STUFF C1094 10UF 20% 4V X6S 0402	NO STUFF C1095 10UF 20% 4V X6S 0402	NO STUFF C1096 10UF 20% 4V X6S 0402	NO STUFF C1097 10UF 20% 4V X6S 0402								
NO STUFF C1022 10UF 20% 4V X6S 0402	NO STUFF C1023 10UF 20% 4V X6S 0402	NO STUFF C1024 10UF 20% 4V X6S 0402	NO STUFF C1025 10UF 20% 4V X6S 0402	NO STUFF C1026 10UF 20% 4V X6S 0402	NO STUFF C1027 10UF 20% 4V X6S 0402	NO STUFF C1028 10UF 20% 4V X6S 0402	NO STUFF C1029 10UF 20% 4V X6S 0402	NO STUFF C1032 10UF 20% 4V X6S 0402	NO STUFF C1033 10UF 20% 4V X6S 0402	NO STUFF C1034 10UF 20% 4V X6S 0402	NO STUFF C1035 10UF 20% 4V X6S 0402	NO STUFF C1036 10UF 20% 4V X6S 0402	NO STUFF C1037 10UF 20% 4V X6S 0402	NO STUFF C1038 10UF 20% 4V X6S 0402						
NO STUFF C1039 10UF 20% 4V X6S 0402	NO STUFF C1044 10UF 20% 4V X6S 0402	NO STUFF C1045 10UF 20% 4V X6S 0402	NO STUFF C1046 10UF 20% 4V X6S 0402	NO STUFF C1047 10UF 20% 4V X6S 0402	NO STUFF C1048 10UF 20% 4V X6S 0402	NO STUFF C1049 10UF 20% 4V X6S 0402															
NO STUFF C1056 10UF 20% 4V X6S 0402	NO STUFF C1057 10UF 20% 4V X6S 0402	NO STUFF C1058 10UF 20% 4V X6S 0402	NO STUFF C1059 10UF 20% 4V X6S 0402	NO STUFF C1062 10UF 20% 4V X6S 0402	NO STUFF C1063 10UF 20% 4V X6S 0402	NO STUFF C1064 10UF 20% 4V X6S 0402	NO STUFF C1065 10UF 20% 4V X6S 0402	NO STUFF C1066 10UF 20% 4V X6S 0402	NO STUFF C1067 10UF 20% 4V X6S 0402	NO STUFF C1068 10UF 20% 4V X6S 0402	NO STUFF C1069 10UF 20% 4V X6S 0402	NO STUFF C1098 10UF 20% 4V X6S 0402	NO STUFF C1099 10UF 20% 4V X6S 0402	NO STUFF C109A 10UF 20% 4V X6S 0402						
NO STUFF C109B 10UF 20% 4V X6S 0402	NO STUFF C109C 10UF 20% 4V X6S 0402	NO STUFF C109D 10UF 20% 4V X6S 0402	NO STUFF C109E 10UF 20% 4V X6S 0402	NO STUFF C109F 10UF 20% 4V X6S 0402	NO STUFF C108A 10UF 20% 4V X6S 0402	NO STUFF C108B 10UF 20% 4V X6S 0402	NO STUFF C108C 10UF 20% 4V X6S 0402	NO STUFF C108D 10UF 20% 4V X6S 0402	NO STUFF C108E 10UF 20% 4V X6S 0402	NO STUFF C108F 10UF 20% 4V X6S 0402	NO STUFF C107A 10UF 20% 4V X6S 0402	NO STUFF C107B 10UF 20% 4V X6S 0402								

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

42 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402 LF	C1041 2.2UF 20% 6.3V CERM 402 LF	C1042 2.2UF 20% 6.3V CERM 402 LF	C1043 2.2UF 20% 6.3V CERM 402 LF

C1050 10UF 20% 6.3V CERM X5R 0402 1	C1051 10UF 20% 6.3V CERM X5R 0402 1	C1052 10UF 20% 6.3V CERM X5R 0402 1	C1053 10UF 20% 6.3V CERM X5R 0402 1	C1054 10UF 20% 6.3V CERM X5R 0402 1	C1055 10UF 20% 6.3V CERM X5R 0402 1

C1060 270UF 20% 2V TANT CASE B2 SM	NO STUFF C1061 270UF 20% 2V TANT CASE B2 SM

2x Bulk nostuff per Harris Beach v1.0 schematic

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH10 6 35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500 Y8 6 35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R CERM 1 603
BYPASS=U0500 AC9 12 7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH11 6 35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500 U8 6 35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH14 6 35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R CERM 1 603
BYPASS=U0500 V8 12 7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500 K14 6 35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R CERM 1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500 AE9 12 7mm
BYPASS=U0500 AE9 6 35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500 J11 12 7mm
BYPASS=U0500 J11 6 35mm
BYPASS=U0500 AE8 6 35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM X5R 0402 1
BYPASS=U0500 K9 6 35mm
BYPASS=U0500 L10 6 35mm
BYPASS=U0500 M9 6 35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500 AG16 6 35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500 J17 6 35mm
BYPASS=U0500 R21 6 35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/10W MF LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM X5R 0805 1
C1271 47UF 20% 4V CERM X5R 0805 1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500 A20 12 7mm
BYPASS=U0500 A20 12 7mm
BYPASS=U0500 A20 6 35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1275 0 5% 1/10W MF LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM X5R 0805 1
C1276 47UF 20% 4V CERM X5R 0805 1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500 J18 12 7mm
BYPASS=U0500 J18 12 7mm
BYPASS=U0500 J18 6 35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

R1280 0 5% 1/10W MF LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
NO STUFF
C1280 47UF 20% 4V CERM X5R 0805 1
NO STUFF
C1281 47UF 20% 4V CERM X5R 0805 1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500 AA21 12 7mm
BYPASS=U0500 AA21 12 7mm
BYPASS=U0500 AA21 6 35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

PP1V05_S0SW_PCH_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
C1290 47UF 20% 4V CERM X5R 0805 1
NO STUFF
C1291 47UF 20% 4V CERM X5R 0805 1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500 B11 12 7mm
BYPASS=U0500 B11 12 7mm
BYPASS=U0500 B11 6 35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
C1295 47UF 20% 4V CERM X5R 0805 1
NO STUFF
C1296 47UF 20% 4V CERM X5R 0805 1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500 B18 12 7mm
BYPASS=U0500 B18 12 7mm
BYPASS=U0500 B18 6 35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

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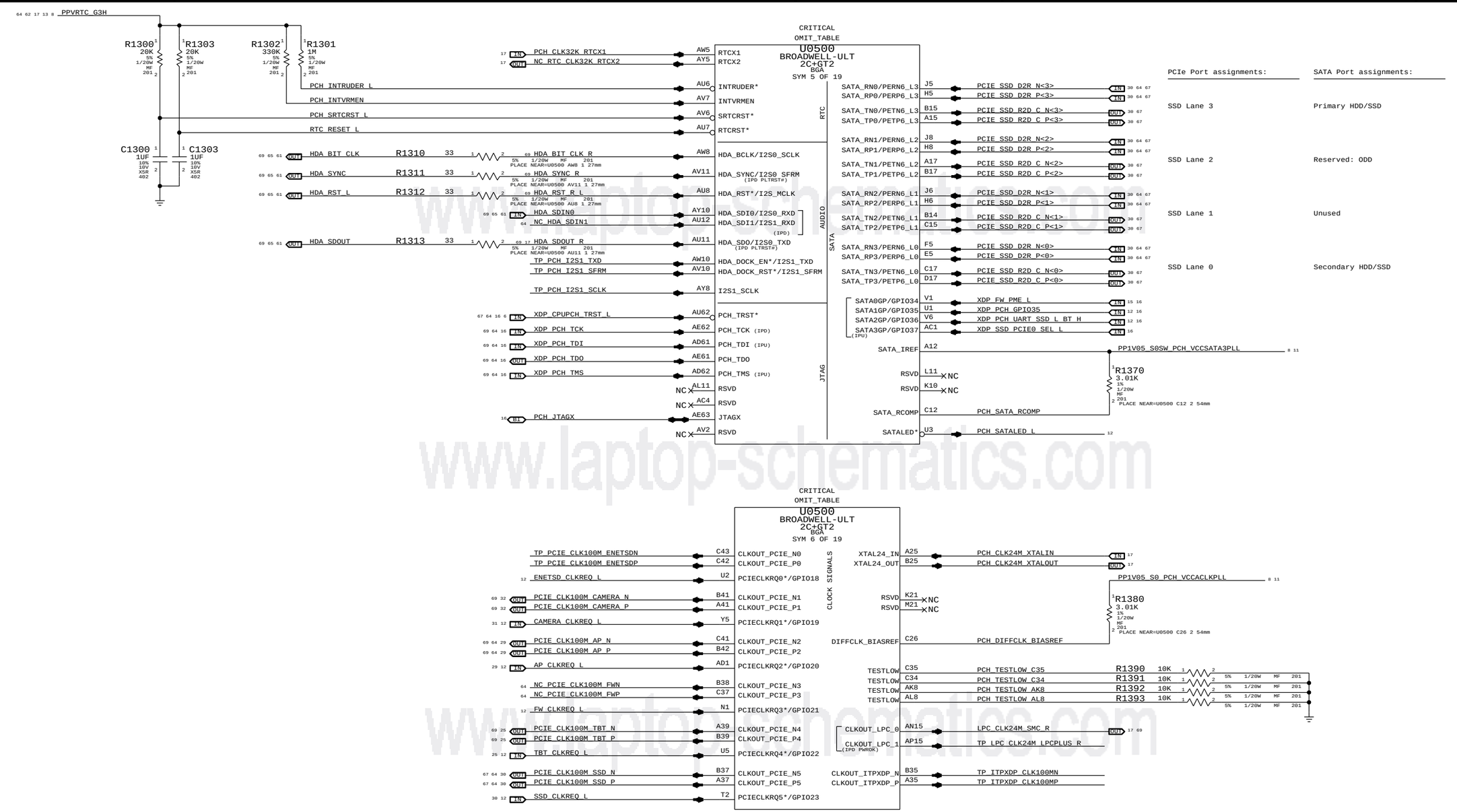

SYNC MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

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SLP_S0# Isolation

PP3V3_S0

C1420 0.1UF 10% 10V X5R CERM 0201

CRITICAL
74LVC1G08 SOT891
U1420 08

PM_SLP_S0_L

NC

SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

R1400 kept for debug purposes.

NO STUFF
R1400 0 5% 1/20W MF 0201

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
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SYSTEM POWER MANAGEMENT

PCH_SUSACK_L	AK2	SUSACK* (IPU)	DSWVRMEN	AW7	PCH_DSWVRMEN
PM_SYSRST_L	AC3	SYS_RESET*	DPWROK	AV5	PM_DSW_PWRGD
PM_PCH_SYS_PWROK	AG2	SYS_PWROK	(IPD DeepSx) WAKE*	AJ5	PCIE_WAKE_L
PM_PCH_PWROK	AY7	PCH_PWROK	CLKRUN*/GPIO32	V5	PM_CLKRUN_L
PM_PCH_PWROK	AB5	APWROK	SUS_STAT*/GPIO61	AG4	LPC_PWRDWN_L
PLT_RESET_L	AG7	PLTRST*	SUSCLK/GPIO62	AE6	PM_CLK32K_SUSCLK_R
PM_RSMRST_L	AW6	RSMRST*	SLP_S5*/GPIO63	AP5	PM_SLP_S5_L
PCH_SUSWARN_L	AV4	SUSWARN*/SUSPWRDNACK/GPIO30	SLP_S4*	AJ6	PM_SLP_S4_L
PM_PWRBTN_L	AL7	PWRBTN* (IPU)	SLP_S3*	AT4	PM_SLP_S3_L
SMC_ADAPTER_EN	AJ8	ACPRESENT/GPIO31 (IPD DeepSx)	SLP_A*	AL5	TP_PM_SLP_A_L
PM_BATLOW_L	AN4	BATLOW*/GPIO72	SLP_SUS*	AP4	PM_SLP_SUS_L
PCH_PM_SLP_S0_L	AF3	SLP_S0*	SLP_LAN*	AJ7	TP_PCH_SLP_LAN_L
TP_PCH_SLP_WLAN_L	AM5	SLP_WLAN*/GPIO29			

PPVRTC_G3H
R1450 330K 5% 1/20W MF 201
R1451 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 9 OF 19

EDP_BKLT_PWM	B8	EDP_BKLCTL	eDP SIDEBAND	DDPB_CTRLCLK	B9	DP_TBTSNK0_DDC_CLK
EDP_BKLT_EN	A9	EDP_BKLEN		DDPB_CTRLDATA (IPD PLTRST#)	C9	DP_TBTSNK0_DDC_DATA
EDP_PANEL_PWR	C6	EDP_VDDEN		DDPC_CTRLCLK	D9	DP_TBTSNK1_DDC_CLK
				DDPC_CTRLDATA (IPD PLTRST#)	D11	DP_TBTSNK1_DDC_DATA
TBT_PWR_REQ_L	U6	PIRQA*/GPIO77	DISPLAY			
SMC_RUNTIME_SCI_L	P4	PIRQB*/GPIO78				
HDMITBTMUX_FLAG	N4	PIRQC*/GPIO79				
SSD_BOOT	N2	PIRQD*/GPIO80				
				DDPB_AUXN	C5	DP_TBTSNK0_AUXCH_C_N
				DDPC_AUXN	B6	DP_TBTSNK1_AUXCH_C_N
				DDPB_AUXP	B5	DP_TBTSNK0_AUXCH_C_P
				DDPC_AUXP	A6	DP_TBTSNK1_AUXCH_C_P
NC_PCI_PME_L	AD4	PME* (IPU)	PCI			
ODD_PWR_EN_L	U7	GPIO55				
HDMITBTMUX_LATCH	L1	GPIO52				
ENET_LOW_PWR	L3	GPIO54				
AUD_PWR_EN	R5	GPIO51				
AP_PCIE_DEV_WAKE	L4	GPIO53				
				DDPB_HPD	C8	DP_TBTSNK0_HPD
				DDPC_HPD	A8	DP_TBTSNK1_HPD
				EDP_HPD	D6	DP_INT_HPD

PP3V3_S5
PP3V3_S0

R1405	1K	PM_PWRBTN_L	13 16 37
R1410	10K	PM_BATLOW_L	13 27 37
R1452	10K	PCIE_WAKE_L	13 29 31 64
R1455	10K	PM_CLKRUN_L	13 37 64
R1460	100K	PM_SLP_S5_L	13 37 59
R1461	100K	PM_SLP_S4_L	13 18 29 36 37 59
R1462	100K	PM_SLP_S3_L	13 17 18 37 59
R1463	100K	PM_SLP_S0_L	13 18 37
R1464	100K	PM_SLP_SUS_L	13 42 59
R1430	100K	EDP_BKLT_EN	13 56
R1431	100K	EDP_PANEL_PWR	13 60
R1440	100K	TBT_PWR_REQ_L	13 26
R1441	100K	SMC_RUNTIME_SCI_L	13 37
R1442	100K	HDMITBTMUX_FLAG	13 64
R1443	100K	SSD_BOOT	13 30
R1445	100K	ODD_PWR_EN_L	13 64
R1446	100K	HDMITBTMUX_LATCH	13 64
R1447	100K	ENET_LOW_PWR	13 64
R1448	100K	AUD_PWR_EN	13 59 61 65
R1449	100K	AP_PCIE_DEV_WAKE	13 64

All: 5% 1/20W MF 201

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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 11 OF 19

69 25 IN	PCIE_TBT_D2R_N<0>	F10	PERN5_L0	
69 25 IN	PCIE_TBT_D2R_P<0>	E10	PERP5_L0	
69 25 OUT	PCIE_TBT_R2D_C_N<0>	C23	PETN5_L0	
69 25 OUT	PCIE_TBT_R2D_C_P<0>	C22	PETP5_L0	
69 25 IN	PCIE_TBT_D2R_N<1>	F8	PERN5_L1	
69 25 IN	PCIE_TBT_D2R_P<1>	E8	PERP5_L1	
69 25 OUT	PCIE_TBT_R2D_C_N<1>	B23	PETN5_L1	
69 25 OUT	PCIE_TBT_R2D_C_P<1>	A23	PETP5_L1	
69 25 IN	PCIE_TBT_D2R_N<2>	H10	PERN5_L2	
69 25 IN	PCIE_TBT_D2R_P<2>	G10	PERP5_L2	
69 25 OUT	PCIE_TBT_R2D_C_N<2>	B21	PETN5_L2	
69 25 OUT	PCIE_TBT_R2D_C_P<2>	C21	PETP5_L2	
69 25 IN	PCIE_TBT_D2R_N<3>	E6	PERN5_L3	
69 25 IN	PCIE_TBT_D2R_P<3>	F6	PERP5_L3	
69 25 OUT	PCIE_TBT_R2D_C_N<3>	B22	PETN5_L3	
69 25 OUT	PCIE_TBT_R2D_C_P<3>	A21	PETP5_L3	
69 64 29 IN	PCIE_AP_D2R_N	G11	PERN3	
69 64 29 IN	PCIE_AP_D2R_P	F11	PERP3	
69 29 OUT	PCIE_AP_R2D_C_N	C29	PETN3	
69 29 OUT	PCIE_AP_R2D_C_P	B30	PETP3	
64	NC_PCIE_FW_D2RN	F13	PERN4	
64	NC_PCIE_FW_D2RP	G13	PERP4	
64	NC_PCIE_FW_R2D_CN	B29	PETN4	
64	NC_PCIE_FW_R2D_CP	A29	PETP4	
68 65 34 IN	USB3_SD_D2R_N	G17	PERN1/USB3RN3	
68 65 34 IN	USB3_SD_D2R_P	F17	PERP1/USB3RP3	
68 65 34 OUT	USB3_SD_R2D_C_N	C30	PETN1/USB3TN3	
68 65 34 OUT	USB3_SD_R2D_C_P	C31	PETP1/USB3TP3	
69 32 IN	PCIE_CAMERA_D2R_N	F15	PERN2/USB3RN4	
69 32 IN	PCIE_CAMERA_D2R_P	G15	PERP2/USB3RP4	
69 32 OUT	PCIE_CAMERA_R2D_C_N	B31	PETN2/USB3TN4	
69 32 OUT	PCIE_CAMERA_R2D_C_P	A31	PETP2/USB3TP4	
NC		E15	RSVD	
NC		E13	RSVD	
	PCH_PCIE_RCOMP	A27	PCIE_RCOMP	
		B27	PCIE_IREF	

PCI-E / USB

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB2N0	AN8	USB_EXTA_N	BI	35 68
USB2P0	AM8	USB_EXTA_P	BI	35 68
USB2N1	AR7	USB_EXTB_N	BI	61 65 68
USB2P1	AT7	USB_EXTB_P	BI	61 65 68
USB2N2	AR8	USB_BT_N	BI	29 68
USB2P2	AP8	USB_BT_P	BI	29 68
USB2N3	AR10	NC_USB_IRN	BI	64
USB2P3	AT10	NC_USB_IRP	BI	64
USB2N4	AM15	USB_TPAD_N	BI	36 64 68
USB2P4	AL15	USB_TPAD_P	BI	36 64 68
USB2N5	AM13	TP_USB_5N		
USB2P5	AN13	TP_USB_5P		
USB2N6	AP11	NC_USB_CAMERAN		64
USB2P6	AN11	NC_USB_CAMERAP		64
USB2N7	AR13	NC_USB_SDN		64
USB2P7 (IPD)	AP13	NC_USB_SDP		64

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

USB3RN1	G20	USB3_EXTA_D2R_N	IN	35 68
USB3RP1	H20	USB3_EXTA_D2R_P	IN	35 68
USB3TN1	C33	USB3_EXTA_R2D_C_N	OUT	35 68
USB3TP1	B34	USB3_EXTA_R2D_C_P	OUT	35 68
USB3RN2	E18	USB3_EXTB_D2R_N	IN	61 65 68
USB3RP2	F18	USB3_EXTB_D2R_P	IN	61 65 68
USB3TN2	B33	USB3_EXTB_R2D_C_N	OUT	61 65 68
USB3TP2	A33	USB3_EXTB_R2D_C_P	OUT	61 65 68

USBRBIAS*	AJ10	PCH_USB_RBIAS	68	
USBRBIAS	AJ11			
RSVD	AN10	NC		
RSVD	AM10	NC		
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L	IN	14 16 35
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L	IN	14 16 61 65
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L	IN	14 16
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L	IN	14 16

PLACE NEAR=U0500.AJ10 2 54mm
R1570 22.6 1% 1/20W MF 201

11 8 PP1V05_S0SW_PCH_VCCUSB3PLL

R1500 3.01K 1% 1/20W MF 201
PLACE NEAR=U0500.A27 2 54mm

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 7 OF 19

69 64 37 BI	LPC_AD<0>	R1540 33	LPC_AD_R<0>	AU14
69 64 37 BI	LPC_AD<1>	R1541 33	LPC_AD_R<1>	AW12
69 64 37 BI	LPC_AD<2>	R1542 33	LPC_AD_R<2>	AY12
69 64 37 BI	LPC_AD<3>	R1543 33	LPC_AD_R<3>	AW11
69 64 37 OUT	LPC_FRAME_L	R1544 33	LPC_FRAME_R_L	AV12
69 46 OUT	SPI_CLK_R			AA3
69 46 OUT	SPI_CS0_R_L			Y7
	TP_SPI_CS1_L			Y4
	TP_SPI_CS2_L			AC2
69 46 BI	SPI_MOSI_R			AA2
69 46 BI	SPI_MISO			AA4
69 46 14 BI	SPI_IO<2>			Y6
69 46 14 BI	SPI_IO<3>			AF1

(IPU)	LAD0			
	LAD1			
	LAD2			
	LAD3			
	LFRAME*			
	SPI_CLK (IPU)			
	SPI_CS0* (IPU)			
	SPI_CS1* (IPU)			
	SPI_CS2* (IPU)			
	SPI_MOSI (IPU/IPD)			
	SPI_MISO (IPU)			
	SPI_IO2 (IPU)			
	SPI_IO3 (IPU)			

LPC / SMBUS / SPI / C-LINK

	SMBALERT*/GPIO11	AN2	PCH_SMBALERT_L	14
	SMBCLK	AP2	SMBUS_PCH_CLK	OUT 16 19 40 56 69
	SMBDATA	AH1	SMBUS_PCH_DATA	BI 16 19 40 56 69
	SML0ALERT*/GPIO60	AL2	WOL_EN	OUT 14 64
	SML0CLK	AN1	SML_PCH_0_CLK	OUT 40 69
	SML0DATA	AK1	SML_PCH_0_DATA	BI 40 69
	SML1ALERT*/PCHHOT*/GPIO73	AU4	PCH_SML1ALERT_L	OUT 18 39
	SML1CLK_GPIO75	AU3	SMBUS_SMC_1_S0_SCL	OUT 32 37 40 43 44 64 69 73
	SML1DATA/GPIO74	AH3	SMBUS_SMC_1_S0_SDA	BI 32 37 40 43 44 64 69 73
(IPU/IPD)	CL_CLK	AF2	NC_CLINK_CLK	64
(IPU/IPD)	CL_DATA	AD2	NC_CLINK_DATA	64
	CL_RST*	AF4	NC_CLINK_RESET_L	64

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS 8 11 14 18 46 57 58 59 62 64
PP3V3_SUS 8 11 14 18 46 57 58 59 62 64

R1580	100K	XDP_USB_EXTA_OC_L		14 16 35
R1581	100K	XDP_USB_EXTB_OC_L		14 16 61 65
R1582	100K	XDP_USB_EXTC_OC_L		14 16
R1583	100K	XDP_USB_EXTD_OC_L		14 16
R1548	1K	SPI_IO<2>		14 46 69
R1549	1K	SPI_IO<3>		14 46 69
R1590	100K	PCH_SMBALERT_L		14
R1591	100K	WOL_EN		14 64

All: 5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201

RAMCFG2:H R1636 100K 5% 1/20W MF 201

RAMCFG1:H R1635 100K 5% 1/20W MF 201

RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PP3V3_S3

SSD_LPSR:S3 R1696 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT 2C+GT2
BGA
SYM 10 OF 19

P1	BMBUSY*/GPIO76	XDP_PCH_GPIO76
AU2	GPIO8	XDP_MLB_RAMCFG0
AM7	LAN_PHY_PWR_CTRL/GPIO12	HDMITBTMUX_SEL_TBT
AD6	GPIO15 (IPD RSMRST#)	TP_MEM_VDD_SEL_1V5_L
Y1	GPIO16	XDP_LPCPLUS_GPIO
T3	GPIO17	XDP_PCH_GPIO17
AD5	GPIO24	SD_RESET_L
AN5	GPIO27 (IPD DeepSx)	SMC_WAKE_SCI_L
AD7	GPIO28	TPAD_SPI_INT_GPIO28_L
AN3	GPIO26	TPAD_USB_IF_EN
AG6	GPIO56	SSD_PWR_EN
AP1	GPIO57	PCH_TBT_PCIE_RESET_L
AL4	GPIO58	HDD_PWR_EN
AT5	GPIO59	XDP_SDCONN_STATE_CHANGE_L
AK4	GPIO44	SD_PWR_EN
AB6	GPIO47	TBT_PWR_EN
U4	GPIO48	XDP_JTAG_ISP_TCK
Y3	GPIO49	XDP_JTAG_ISP_TDI
P3	GPIO50	JTAG_TBT_TMS_PCH
Y2	HSIOPC/GPIO71	PCH_HSIO_PWR_EN
AT3	GPIO13	TPAD_SPI_IF_EN
AH4	GPIO14	XDP_MLB_RAMCFG3
AM4	GPIO25	SPIROM_USE_MLB
AG5	GPIO45	CAMERA_PWR_EN_PCH
AG3	GPIO46	TPAD_SPI_INT_GPIO46_L
AM3	GPIO9	XDP_MLB_RAMCFG1
AM2	GPIO10	XDP_MLB_RAMCFG2
P2	DEVSLP0/GPIO33	SSD_SR_EN_L
C4	SDIO_POWER_EN/GPIO70	AP_S0IX_WAKE_SEL
L2	DEVSLP1/GPIO38	SSD_RESET_L
N5	DEVSLP2/GPIO39	CAM_PCIE_RESET_L
V2	SPKR/GPIO81 (IPD PLTRST#)	PCH_TCO_TIMER_DISABLE

CPU/MISC

D60	THERMTRIP*	PM_THRMTRIP_L
V4	RCIN*/GPIO82	TBT_CIO_PLUG_EVENT_L
T4	SERIRQ	LPC_SERIRQ
AW15	PCH_OPI_COMP	PCH_OPI_COMP
AF20	RSVD	NC
AB21	RSVD	NC

GPIO / LPIO

R6	GSPI0_CS*/GPIO83	AUD_SPI_CS_L
L6	GSPI0_CLK/GPIO84	AUD_SPI_CLK
N6	GSPI0_MISO/GPIO85 (IPD)	AUD_SPI_MISO
L8	GSPI0_MOSI/GPIO86 (IPD PLTRST#)	AUD_SPI_MOSI
R7	GSPI1_CS*/GPIO87	TPAD_SPI_CS_L
L5	GSPI1_CLK/GPIO88	TPAD_SPI_CLK
N7	GSPI1_MISO/GPIO89 (IPD)	TPAD_SPI_MISO
K2	GSPI_MOSI/GPIO90	TPAD_SPI_MOSI
J1	UART0_RXD/GPIO91	PCH_BT_UART_D2R
K3	UART0_TXD/GPIO92	PCH_BT_UART_R2D
J2	UART0_RTS*/GPIO93	PCH_BT_UART_RTS_L
G1	UART0_CTS*/GPIO94	PCH_BT_UART_CTS_L
K4	UART1_RXD/GPIO0	PCH_UART1_RXD
G2	UART1_TXD/GPIO1	PCH_UART1_TXD
J3	UART1_RST*/GPIO2	JTAG_ISP_TDO
J4	UART1_CTS*/GPIO3	PCH_UART1_CTS_L
F2	I2C0_SDA/GPIO4	AP_S0IX_WAKE_L
F3	I2C0_SCL/GPIO5	AP_RESET_L
G4	I2C1_SDA/GPIO6	PCH_I2C1_SDA
F1	I2C1_SCL/GPIO7	PCH_I2C1_SCL
E3	SDIO_CLK/GPIO64	TBT_POC_RESET_L
F4	SDIO_CMD/GPIO65	BT_PWRRST_L
D3	SDIO_D0/GPIO66 (IPD PLTRST#)	PCH_STRP_TOPBLK_SWP_L
E4	SDIO_D1/GPIO67	ENET_MEDIA_SENSE
C3	SDIO_D2/GPIO68	LCD_IRQ_L
E2	SDIO_D3/GPIO69	LCD_PSR_EN

PP1V05_S0

R1650 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15.2.54mm
R1655 49.9 1% 1/20W MF 201

PLT_RESET_L

R1621 100K 5% 1/20W MF 201

TPAD_SPI_INT_GPIO28_L

R1681 0 5% 1/20W MF 0201

TPAD_SPI_INT_L

R1682 0 5% 1/20W MF 0201

TPAD_SPI_INT_GPIO46_L

R1639 100K 5% 1/20W MF 201

R1680 100K 5% 1/20W MF 201

SSD_RESET_L

CAM_PCIE_RESET_L

PP3V3_S0

R1641 1K 5% 1/20W MF 201

PCH_TCO_TIMER_DISABLE

PLT_RESET_L

R1671 100K 5% 1/20W MF 201

AP_RESET_L

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S5
PP3V3_S3
PP3V3_S0SW_SD
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_S0

TBTLC for CR, S0 for RR

R1610	100K	XDP_PCH_GPIO76	
R1614	100K	XDP_LPCPLUS_GPIO	
R1615	100K	XDP_PCH_GPIO17	
SD_ON_MLB			
R1616	100K	SD_RESET_L	R1616 should also be stuffed if platform does not use SD card
R1617	100K	SMC_WAKE_SCI_L	
R1618	100K	TPAD_SPI_INT_L	
R1619	100K	TPAD_USB_IF_EN	
R1620	100K	SSD_PWR_EN	SSD_LPSR:S0 BOM option is on R1620
SSD_LPSR:S0			
R1622	100K	HDD_PWR_EN	
R1623	100K	XDP_SDCONN_STATE_CHANGE_L	
R1624	100K	SD_PWR_EN	
R1625	100K	TBT_PWR_EN	
R1626	100K	XDP_JTAG_ISP_TCK	
R1627	100K	XDP_JTAG_ISP_TDI	
R1628	100K	JTAG_TBT_TMS_PCH	
R1629	100K	PCH_HSIO_PWR_EN	
R1630	100K	TPAD_SPI_IF_EN	
R1632	100K	SPIROM_USE_MLB	Stuffed R1632
R1633	100K	CAMERA_PWR_EN_PCH	
R1634	100K	TPAD_SPI_INT_GPIO46_L	No-Stuffed R1634
NOSTUFF			
R1637	100K	SSD_SR_EN_L	
R1638	100K	AP_S0IX_WAKE_SEL	
R1640	100K	XDP_FW_PME_L	
R1652	10K	LPC_SERIRQ	
R1691	100K	BT_PWRRST_L	
R1693	100K	ENET_MEDIA_SENSE	
R1694	100K	LCD_IRQ_L	
R1695	100K	LCD_PSR_EN	

PP3V3_S0

AUD_SPI_CS_L	R1660	100K	
AUD_SPI_CLK	R1661	100K	
AUD_SPI_MISO	R1662	100K	
AUD_SPI_MOSI	R1663	100K	
TPAD_SPI_CS_L	R1664	47K	
TPAD_SPI_CLK	R1665	47K	
TPAD_SPI_MISO	R1666	47K	
TPAD_SPI_MOSI	R1667	47K	
PCH_BT_UART_D2R	R1668	47K	
PCH_BT_UART_R2D	R1669	47K	
PCH_UART1_RXD	R1672	47K	
PCH_UART1_TXD	R1673	47K	
JTAG_ISP_TDO	R1674	100K	
PCH_UART1_CTS_L	R1675	47K	
AP_S0IX_WAKE_L	R1676	100K	
PCH_I2C1_SDA	R1678	2.2K	
PCH_I2C1_SCL	R1679	2.2K	
PCH_BT_UART_RTS_L	R1670	47K	
PCH_BT_UART_CTS_L	R1677	47K	

SYNC_MASTER=WILL_J43 SYNC_DATE=01/14/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP P6)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M ST SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

R1830 150 5% 1/16W MF LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0 → CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1 → CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0 → CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1 → CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2 → CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3 → CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0 → CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1 → CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0 → CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1 → CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2 → CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3 → CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 → NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 → NC
VCC_OBS_AB	HOOK2	VCC_OBS_CD
CPU_PWR_DEBUG	HOOK3	RESET#/HOOK6 ← XDP_CPURST_L
SMBUS_PCH_DATA	SDA	DBR#/HOOK7 ← XDP_DBRESET_L
SMBUS_PCH_CLK	SCL	TDO → XDP_PCH_TDO
XDP_PCH_TCK	TCK1	TRSTn ← XDP_TRST_L
XDP_SYS_PWROK	TCK0	TDI ← XDP_PCH_TDI
		TMS ← XDP_PCH_TMS
		XDP_PRESENT# → XDP_CPU_PRESENT_L

518S0847

XDP C1804 0.1UF 10% 6.3V CERM X5R 0201
XDP R1831 1K 5% 1/16W MF LF 402
XDP C1800 0.1UF 10% 6.3V CERM X5R 0201
XDP C1801 0.1UF 10% 6.3V CERM X5R 0201
XDP C1806 0.1UF 10% 6.3V CERM X5R 0201

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP R1805 1K 5% 1/20W MF 201 — PLT_RESET_L
PLACE NEAR=U0500 AG7 Z 54mm

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL XDP Q1840 DMN5L06VK-7 SOT563 VER 3
PLACE NEAR=J1800 51 28MM
XDP_CPU_TDO

CRITICAL XDP Q1840 DMN5L06VK-7 SOT563 VER 3
XDP_CPUPCH_TRST_L (MAKE BASE=TRUE)
XDP_CPUPCH_TRST_L
XDP_CPUPCH_TRST_L

CRITICAL XDP Q1842 DMN5L06VK-7 SOT563 VER 3
PLACE NEAR=J1800 55 28mm
XDP_CPU_TDI

CRITICAL XDP Q1842 DMN5L06VK-7 SOT563 VER 3
XDP_CPU_TMS

PP1V05_S0

XDP R1810 51 5% 1/20W MF 201 — XDP_CPU_TDO
PLACE NEAR=U0500 F62 28mm

XDP R1813 51 5% 1/20W MF 201 — XDP_CPU_TCK
PLACE NEAR=U0500 E60 28mm

TDI and TMS are terminated in CPU.

CPU_VCCST_PWRGD — XDP R1800 1K 5% 1/20W MF 201 — PLACE NEAR=U0500 C61 2 54mm
PM_PWRBTN_L — XDP R1802 0 5% 1/20W MF 0201 — PLACE NEAR=U5000 J3 2 54mm
PM_PCH_SYS_PWROK — XDP R1804 0 5% 1/16W MF LF 402
XDP_CPU_TCK
PCH_JTAGX — XDP R1835 0 5% 1/20W MF 0201 — PLACE NEAR=J1800 58 28mm

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L		XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L		XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L		XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_FW_PME_L	TP1879	
XDP_PCH_GPIO35	TP1880	
XDP_PCH_UART_SSD_L_BT_H	TP1881	
XDP_SSD_PCIE0_SEL_L — R1884 1K 5% 1/20W MF 201		
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

(MAKE BASE=TRUE, TP P6)

NOTE: Must not short XDP pins together!

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C1845 0.1UF 10% 16V X5R CERM 0201
U1845 74LVC1G07GF SOT891 VCC GND
R1845 330K 5% 1/20W MF 201

NC — NC — NC — NC

XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

(5% 1/20W MF 201)

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenCLK 25MHz Power
Must be powered if any VDDIO is powered.
PP3V3_S5RS3RS0_SYSCLKGEN

CAM XTAL Power
TBT XTAL Power
PP1V2_CAM_XTALPCIEVDD
PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R CERM 0201
C1922 0.1UF 10% 16V X5R CERM 0201
C1902 1UF 20% 6.3V X5R 0201
CKPLUS WAIVE=PwrTerm2Gnd

U1900 SLG3NB148CV TQFN CRITICAL
NC, VDD, VG3HOT
VIOE_25M_A, VIOE_25M_B, VIOE_25M_C
25M_A, 25M_B, 25M_C
GND, THRM PAD

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

32.768K
PCH_CLK32K_RTCX1
NC
SYSCLK_CLK25M_CAMERA
SYSCLK_CLK25M_TBT
PPVRTC_G3H
For SB RTC Power
C1910 1UF 20% 6.3V X5R 0201

C1905 12PF 5% 25V CERM 0201
C1906 12PF 5% 25V CERM 0201
SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
R1905 0 5% 1/20W MF 0201
NO STUFF
R1906 1M 5% 1/20W MF 201
CRITICAL
Y1905 25.000MHZ-12PF-20PPM
SM 3 2X2 5MM
X2
X1
SYSCLK_CLK25M_X1
NOTE: 30 PPM or better required for RTC accuracy

NC_RTC_CLK32K_RTCX2
MAKE BASE=TRUE
NC_RTC_CLK32K_RTCX2
NO TEST=TRUE

PCH 24MHz Crystal

C1915 6.8PF +/- 0.1PF 25V C0G 0201
C1916 6.8PF +/- 0.1PF 25V C0G 0201
PCH_CLK24M_XTALOUT_R
PCH_CLK24M_XTALOUT
R1915 0 5% 1/20W MF 0201
CRITICAL
Y1915 24.000MHZ-20PPM-6PF
3 20X2 50MM SM1
R1916 1M 5% 1/20W MF 201
PCH_CLK24M_XTALIN

PCH 24MHz Outputs

LPC_CLK24M_SMC_R
PLACE NEAR=U0500.AN15 5 1mm
R1927 22 5% 1/20W MF 201
LPC_CLK24M_SMC
MAKE BASE=TRUE
LPC_CLK24M_SMC

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 1/20W 0201 MF 5%
XDP_DBRESET_L
PM_SYSRST_L
NO STUFF
R1997 0 5% 1/16W MF LF 402
SILK PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
C1970 0.1UF 10% 16V X5R CERM 0201
U1970 74AUP1G07GF SOT891
VCC, A, NC, NC, GND, NC, Y, NC
PP3V3_S0
R1970 330K 5% 1/20W MF 201
TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low
CPU_MEMVTT_PWR_EN_LSVDDQ
MEMVTT_PWR_EN
MAKE BASE=TRUE
MEMVTT_PWR_EN

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201
Q1920 DMN5L06VK-7 SOT563 VER 3
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE
Q1920 DMN5L06VK-7 SOT563 VER 3
R1921 1K 5% 1/20W MF 201
HDA_SDOUT_R
IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R CERM 0201
CRITICAL
U1930 74AUP1G09 SOT891
VCC, A, B, NC, GND, Y
PP1V05_S0
R1931 10K 5% 1/20W MF 201
ALL_SYS_PWRGD
PM_SLP_S3_L
CPU_VCCST_PWRGD

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
BYPASS=U1950 5MM
C1950 0.1UF 10% 16V X5R CERM 0201
R1950 10K 5% 1/20W MF 201
CPU_VR_EN
R1955 10K 5% 1/20W MF 201
NO STUFF
R1951 0 5% 1/20W MF 0201
CPU_VR_READY
MAKE BASE=TRUE
CPU_VR_READY
ALL_SYS_PWRGD
CPUVR_PGOOD_R
U1950 74LVC2G08GT/SS05 SOT833
PM_S0_PGOOD
R1963 0 5% 1/20W MF 0201
NO STUFF
R1960 0 5% 1/20W MF 0201
WF: Do we need this?
CKPLUS WAIVE=UNCONNECTED PINS
NO STUFF
R1961 100K 5% 1/20W MF 201
U1950 74LVC2G08GT/SS05 SOT833
SYS_PWROK_R
R1962 1K 5% 1/20W MF 201
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_PWROK
MAKE BASE=TRUE
SMC_DELAYED_PWRGD

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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Platform Reset Connections

Unbuffered

PLT_RESET_L (IN) → R2071 0 5% 1/20W MF 0201 → PCA9557D_RESET_L (OUT)

Scrub for Layout Optimization

Buffered

PP3V3_S0 → U2071 CRITICAL MC74VHC1G08 SC70 HF
C2071 0.1UF 10% 16V X5R CERM 0201
R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L → R2072 0 → SMC_LRESET_L (OUT)
PLT_RST_BUF_L → R2088 0 → BKLT_PLT_RST_L (OUT)
NOSTUFF R2089 0 → CAM_PCIE_RESET_L (OUT)

PCH_TBT_PCIE_RESET_L (IN, MAKE BASE=TRUE) = PCH_TBT_PCIE_RESET_L (OUT)

PP3V3_S5
NOSTUFF C2030 0.1UF 10% 10V X5R CERM 0201 (BYPASS=U2030 3mm)
NOSTUFF CRITICAL U2030 74LVC1G08 SOT891
PM_SLP_S4_L (IN) → U2030
CAMERA_PWR_EN_PCH (IN) → U2030 → CAMERA_PWR_EN (OUT)
U2030 NC
R2030 0 5% 1/20W MF 0201

Power State Debug LEDs

(For development only)

PP3V3_S5 → R2094 0 5% 1/10W MF LF 402 (PLACE SIDE=BOTTOM) → PP3V3_S5_DBGLED (MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 25 MM, VOLTAGE=3 3V)

R	D	Q	Signal
R2090 20K	D2090 GREEN 56MCD 2MA 2 65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S5 ON		DBGLED_S5
R2091 20K	D2091 GREEN 56MCD 2MA 2 65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=STBY ON		DBGLED_S4
R2092 20K	D2092 GREEN 56MCD 2MA 2 65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S3 ON		DBGLED_S3
R2093 20K	D2093 GREEN 56MCD 2MA 2 65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S0I3 ON		DBGLED_S0I3
R2095 20K	D2095 GREEN 56MCD 2MA 2 65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S0 ON		DBGLED_S0
		Q2090 DMN5L06VK-7 SOT563 VER 3	DBGLED_S4_D
		Q2090 DMN5L06VK-7 SOT563 VER 3	DBGLED_S3_D
		Q2091 DMN5L06VK-7 SOT563 VER 3	DBGLED_S0I3_D
		Q2091 DMN5L06VK-7 SOT563 VER 3	DBGLED_S0_D

S4_PWR_EN (IN)
PM_SLP_S4_L (IN)
PM_SLP_S3_L (IN)
PM_SLP_S0_L (IN)

GreenCLK 25MHz Power

NO STUFF R2040 0 5% 1/20W MF 0201: PP3V3_S3 → PP3V3_S5RS3RS0_SYSCLKGEN = PP3V3_S5RS3RS0_SYSCLKGEN (MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 MM, VOLTAGE=3 3V, MAKE BASE=TRUE)

NO STUFF R2041 0 5% 1/20W MF 0201: PP3V3_S0

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

R2042 0 5% 1/20W MF 0201: PP3V3_S5

Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

PP3V3_TBTLC
R2061 100K 5% 1/20W MF 201
C2060 0.1UF 20% 10V CERM 402
R2062 100K 5% 1/20W MF 201
U2060 74LVC2G07 SOT891 (VCC, GND)

From RR / From PCH

JTAG_TBT_TDO (IN) → 1A → 1Y → JTAG_ISP_TDO (OUT) → To PCH
JTAG_TBT_TMS_PCH (IN) → 2A → 2Y → JTAG_TBT_TMS (OUT) → To RR

S0 pull-up on PCH page

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary.

Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property

TP_CPU_RSVDN61 = TP_CPU_RSVDN61 (MAKE BASE=TRUE)
TP_CPU_RSVDP61 = TP_CPU_RSVDP61 (MAKE BASE=TRUE)

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0 (OUT)
XDP_MLB_RAMCFG1 (OUT)
XDP_MLB_RAMCFG2 (OUT)
XDP_MLB_RAMCFG3 (OUT)

RAMCFG3:L	R2050 10K 5% 1/20W MF 201
RAMCFG2:L	R2051 10K 5% 1/20W MF 201
RAMCFG1:L	R2052 10K 5% 1/20W MF 201
RAMCFG0:L	R2053 10K 5% 1/20W MF 201

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L (IN) = TP_CPU_MEM_RESET_L (MAKE BASE=TRUE)
TP_MEM_VDD_SEL_1V5_L (IN) = TP_MEM_VDD_SEL_1V5_L (MAKE BASE=TRUE)
PP0V6_S3_MEM_VREFDQ_A = PP0V6_S3_MEM_VREFDQ_A (MAKE BASE=TRUE, VOLTAGE=0 6V)
PP0V6_S3_MEM_VREFCA_A = PP0V6_S3_MEM_VREFCA_A (MAKE BASE=TRUE, VOLTAGE=0 6V)
PP0V6_S3_MEM_VREFDQ_B = PP0V6_S3_MEM_VREFDQ_B (MAKE BASE=TRUE, VOLTAGE=0 6V)
PP0V6_S3_MEM_VREFCA_B = PP0V6_S3_MEM_VREFCA_B (MAKE BASE=TRUE, VOLTAGE=0 6V)

DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0
NO STUFF R2020 2.2K 5% 1/20W MF 201
R2021 2.2K 5% 1/20W MF 201
NO STUFF R2022 2.2K 5% 1/20W MF 201
R2023 2.2K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

PP3V3_S0
R2015 100K 5% 1/20W MF 201

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC (on TBT page)

HDMITBTMUX_SEL_TBT (BI) = HDMITBTMUX_SEL_TBT (BI) (MAKE BASE, TRUE)

Falcon Ridge PLUG_EVENT is active-low, always driven (pull-up)

TBT_CIO_PLUG_EVENT_L (OUT) = TBT_CIO_PLUG_EVENT_L (IN) (TRUE)

Required for unused second TBT port

TBT_B_CIO_SEL (IN)
DP_TBTPB_HPD (OUT)
TBT_B_CONFIG2_RC (OUT)
TBT_B_CONFIG1_BUF (OUT)
TBT_B_LSRX

R2016 10K, R2017 10K, R2018 10K, R2019 10K, R2014 10K (5% 1/20W MF 201)

TBT Aliases

MAKE BASE

DP_TBTSNK0_DDC_CLK (IN) = DP_TBTSNK0_DDC_CLK (OUT) (TRUE)
DP_TBTSNK0_DDC_DATA (BI) = DP_TBTSNK0_DDC_DATA (BI) (TRUE)

MAKE BASE

DP_TBTSNK1_HPD (OUT) = DP_TBTSNK1_HPD (IN) (TRUE)
=DP_TBTSNK1_ML_C_P<3..0> (IN) = DP_TBTSNK1_ML_C_P<3..0> (OUT) (TRUE)
=DP_TBTSNK1_ML_C_N<3..0> (IN) = DP_TBTSNK1_ML_C_N<3..0> (OUT) (TRUE)
DP_TBTSNK1_AUXCH_C_P (BI) = DP_TBTSNK1_AUXCH_C_P (BI) (TRUE)
DP_TBTSNK1_AUXCH_C_N (BI) = DP_TBTSNK1_AUXCH_C_N (BI) (TRUE)
DP_TBTSNK1_DDC_CLK (IN) = DP_TBTSNK1_DDC_CLK (TRUE)
DP_TBTSNK1_DDC_DATA (BI) = DP_TBTSNK1_DDC_DATA (TRUE)

Single-port TBT implementation does not require DDC Crossbar

XDP_JTAG_ISP_TCK (IN) = XDP_JTAG_ISP_TCK (OUT)
XDP_JTAG_ISP_TDI (IN) = XDP_JTAG_ISP_TDI (OUT)

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

PP3V3_SUS
R2010 100K 5% 1/20W MF 201
PCH_SML1ALERT_L (OUT)

SYNC_MASTER=J43_MLB	SYNC_DATE=01/17/2013
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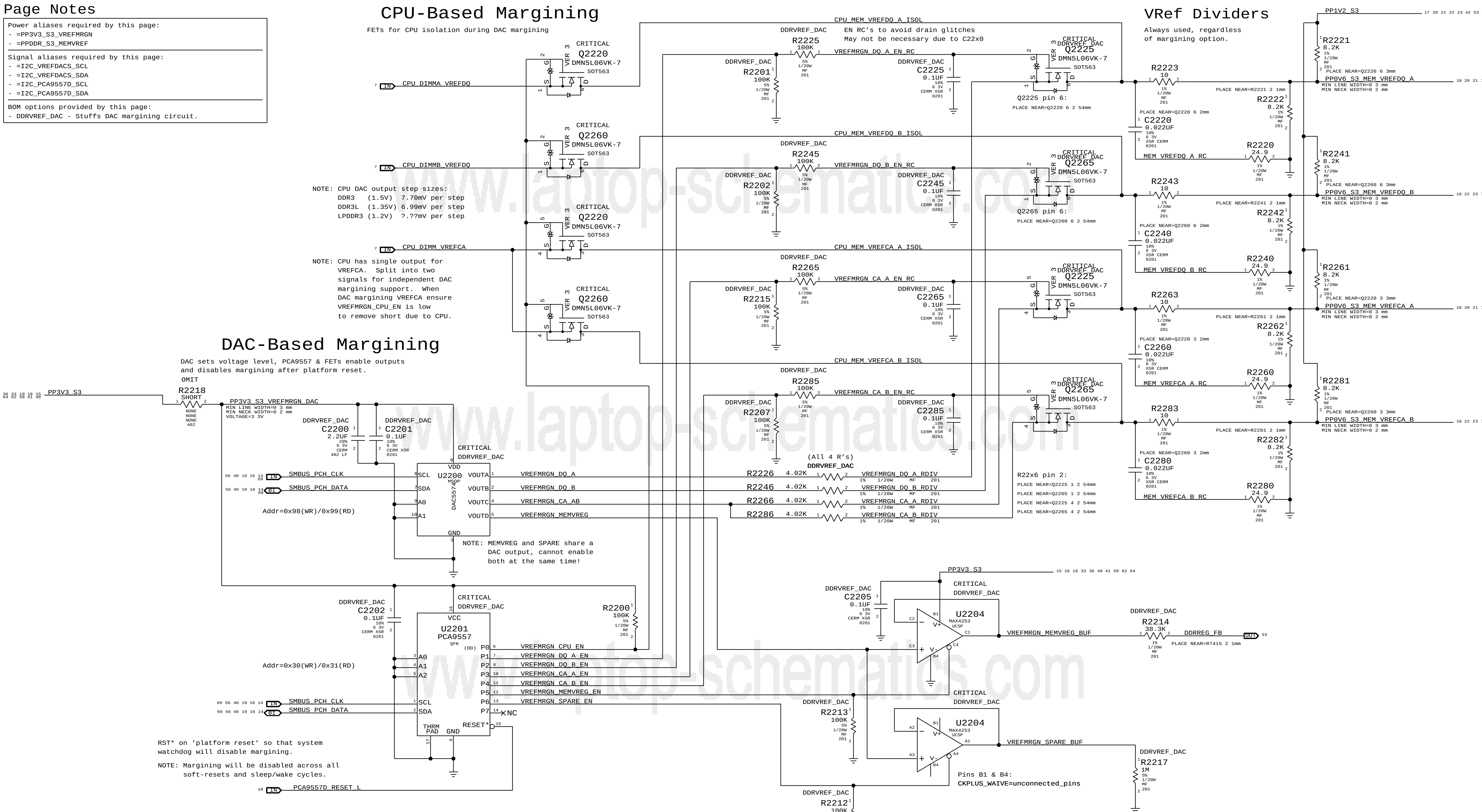


	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	LPDDR3 (1.2V)	DDR3L (1.35V)	LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)	0.675V (DAC: 0x34)	1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)	0.337V - 1.013V (+/- 337.5mV)	0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)	+82uA - -82uA (- = sourced)	+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output	6.36mV / step @ output	4.28mV / step @ output	3.53mV / step @ output

SYNC_MASTER=J41_MLB SYNC_DATE=02/12/2013

PAGE TITLE

DDR3 VREF MARGINING

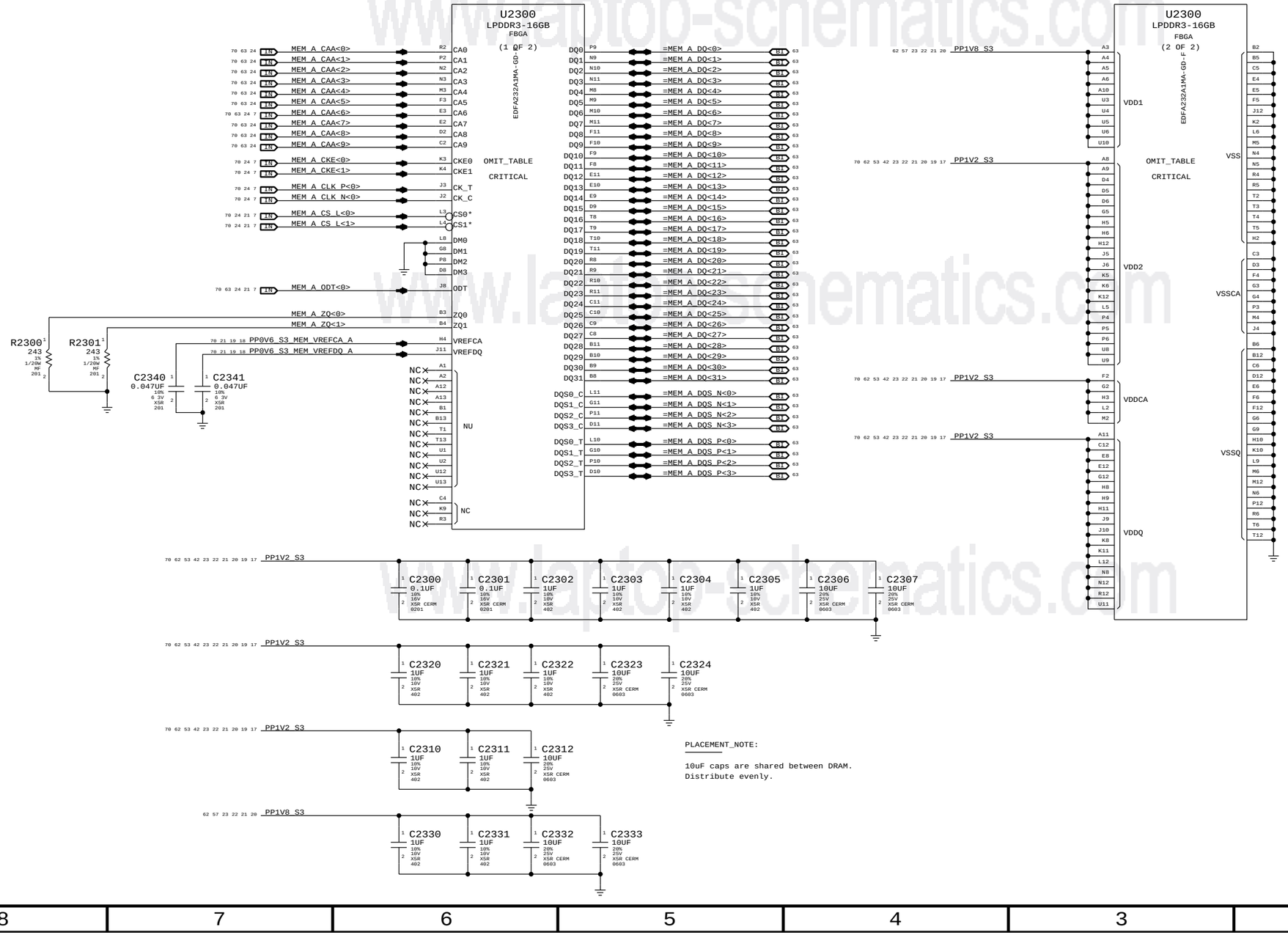
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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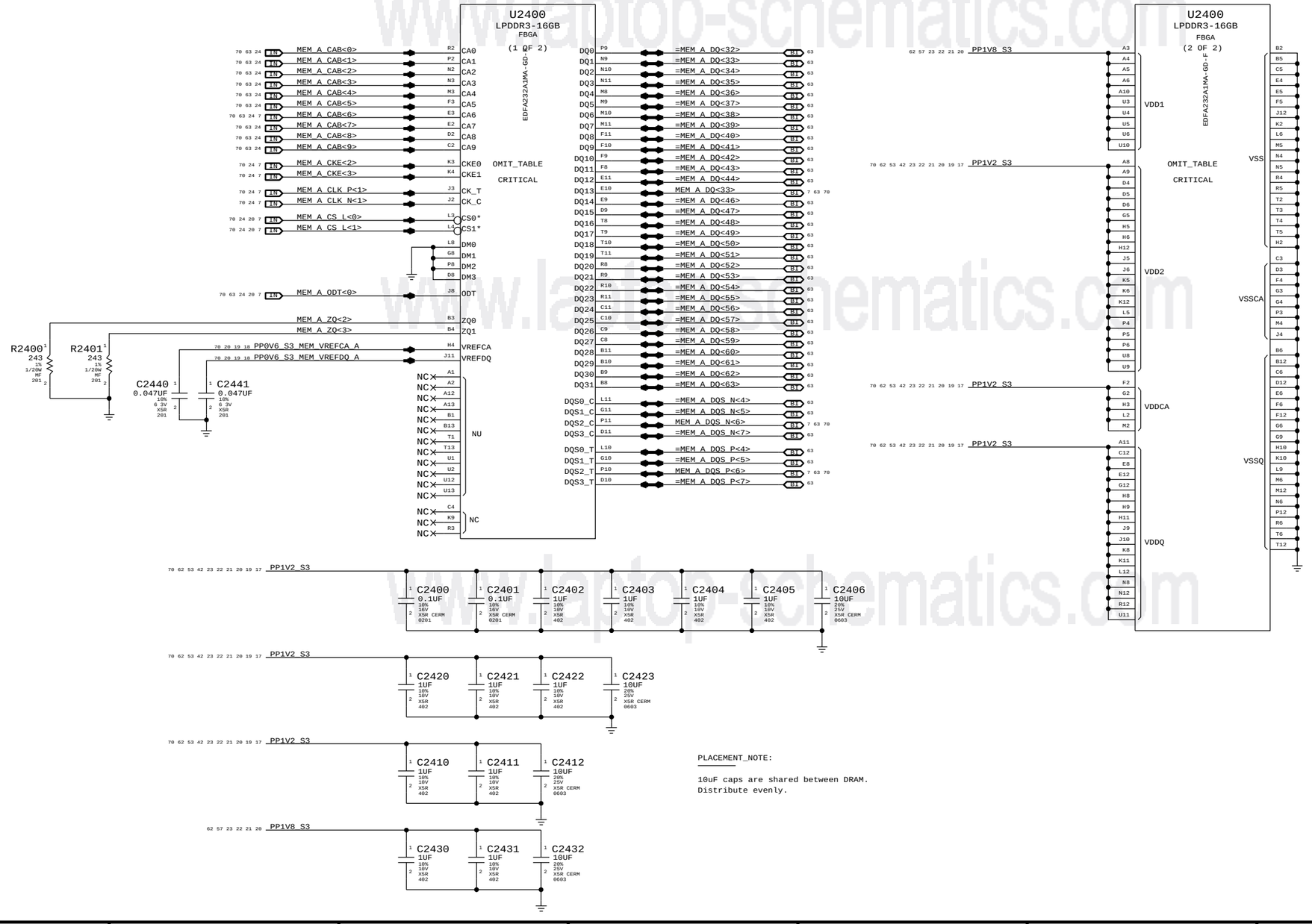
LPDDR3 CHANNEL A (32-63)



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

Apple Inc.

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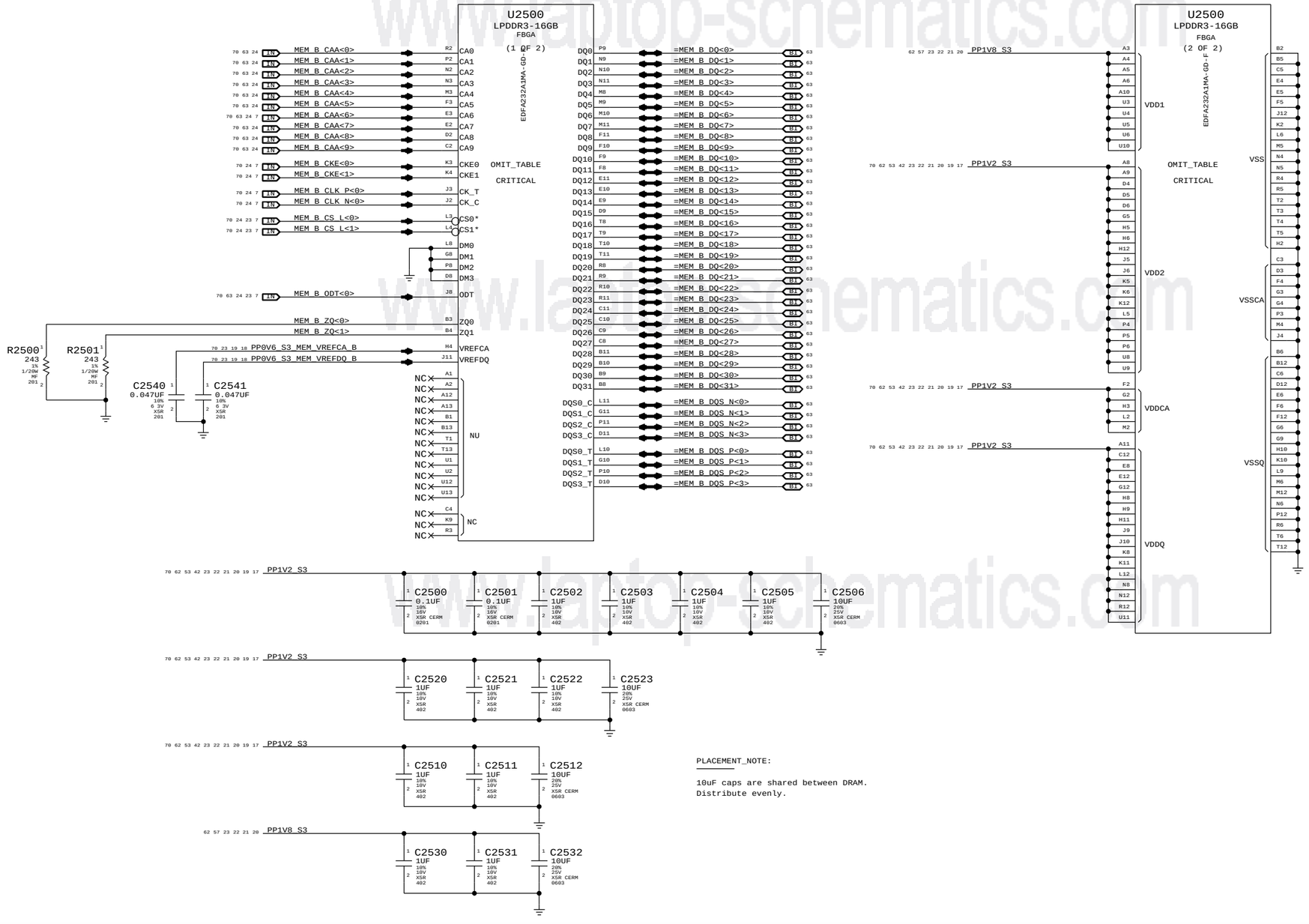
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

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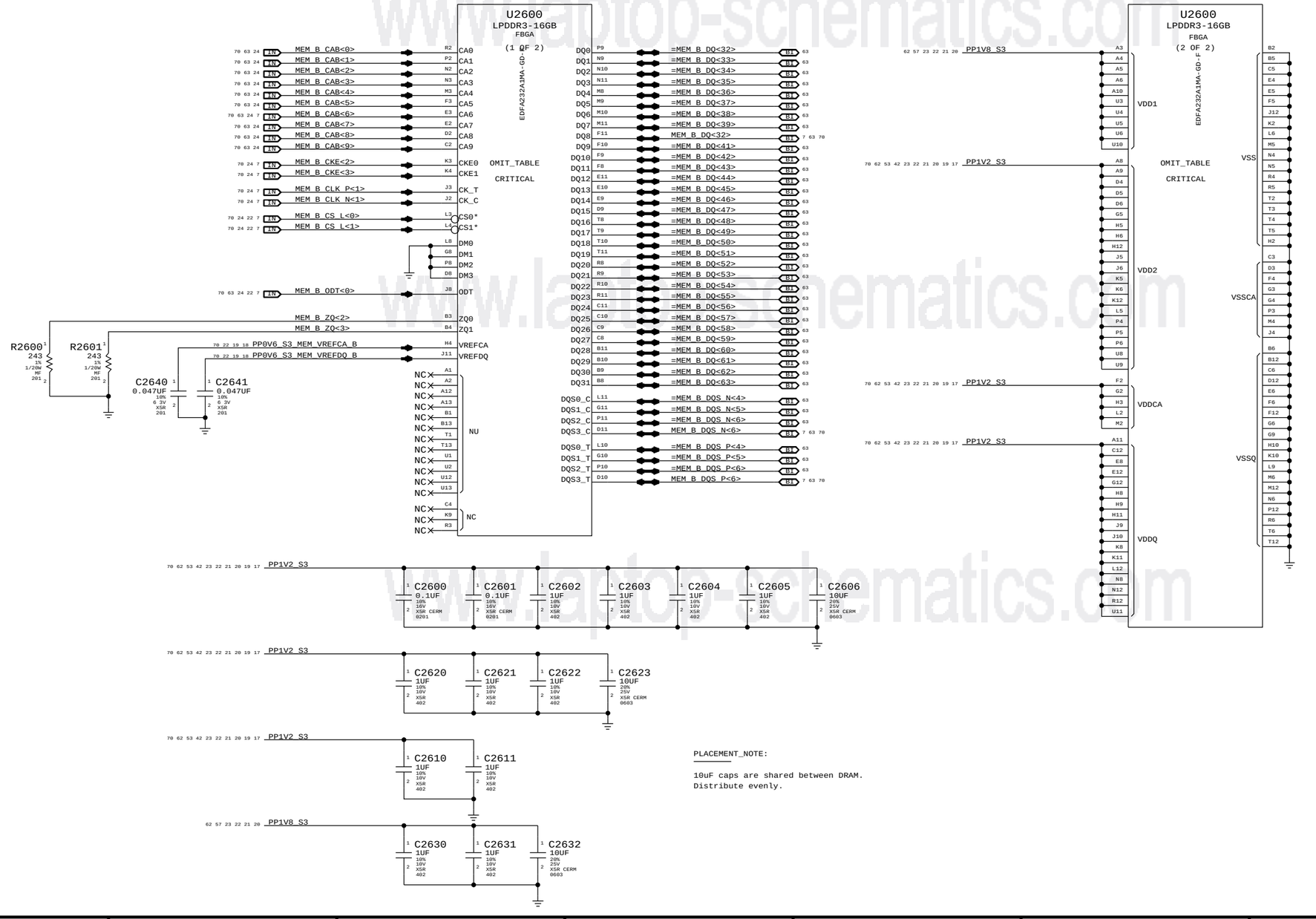
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

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LPDDR3 DRAM Channel B (32-63)

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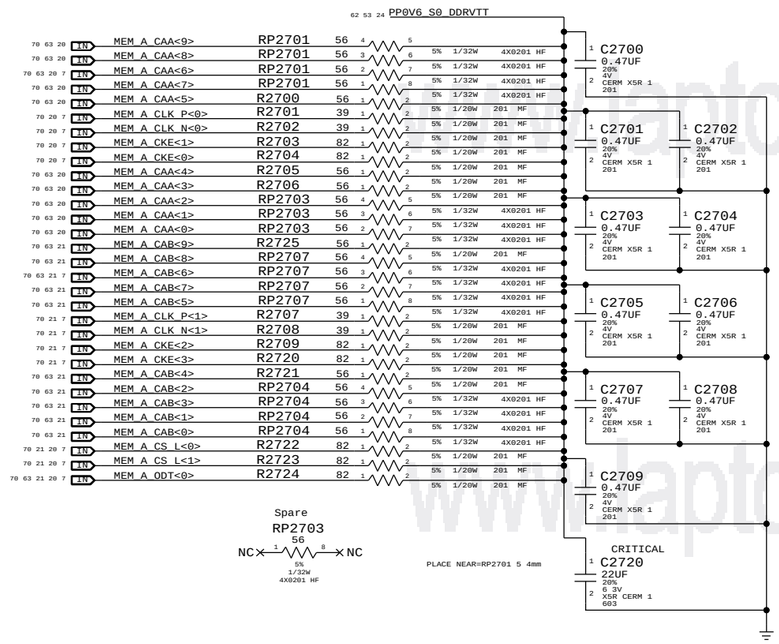
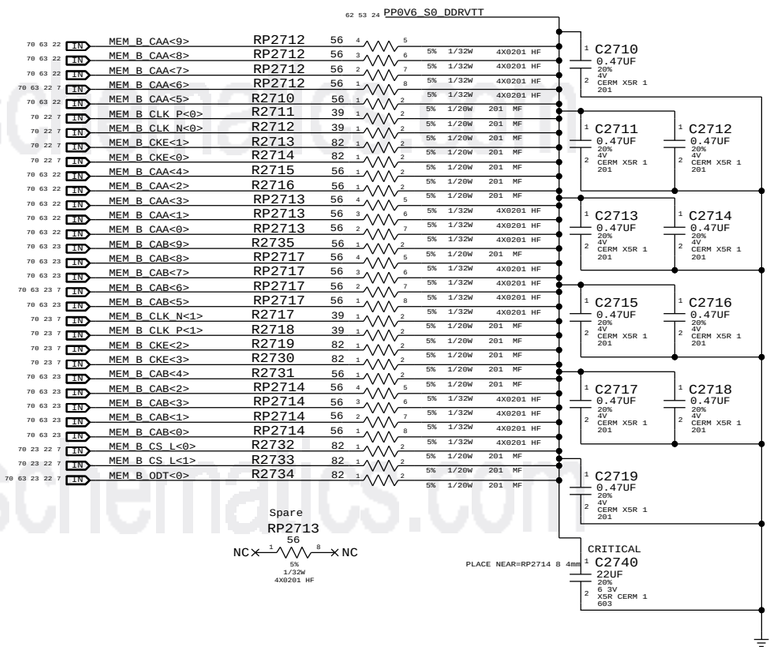
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC MASTER=J41_MLB SYNC DATE=02/06/2013

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

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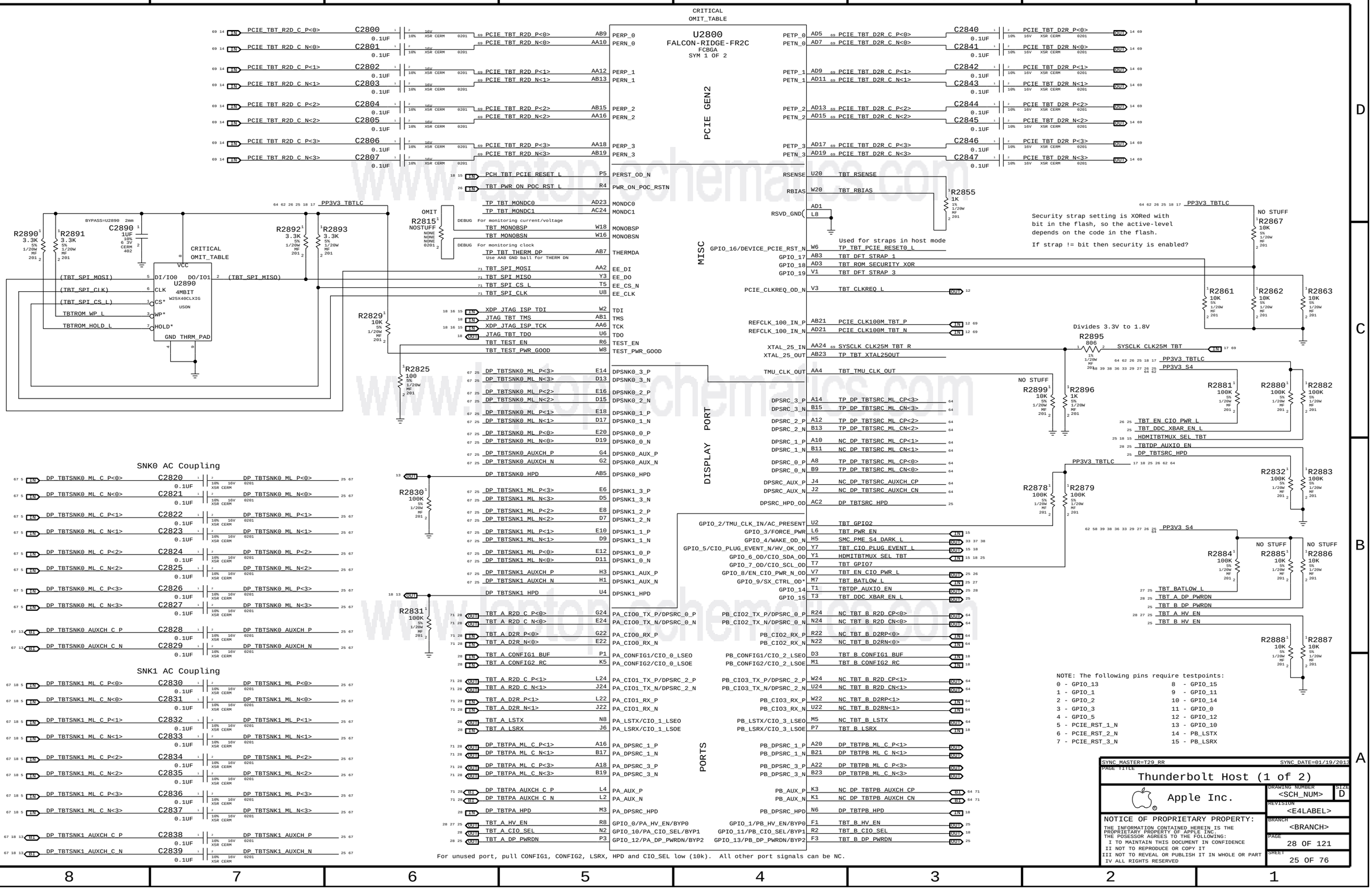

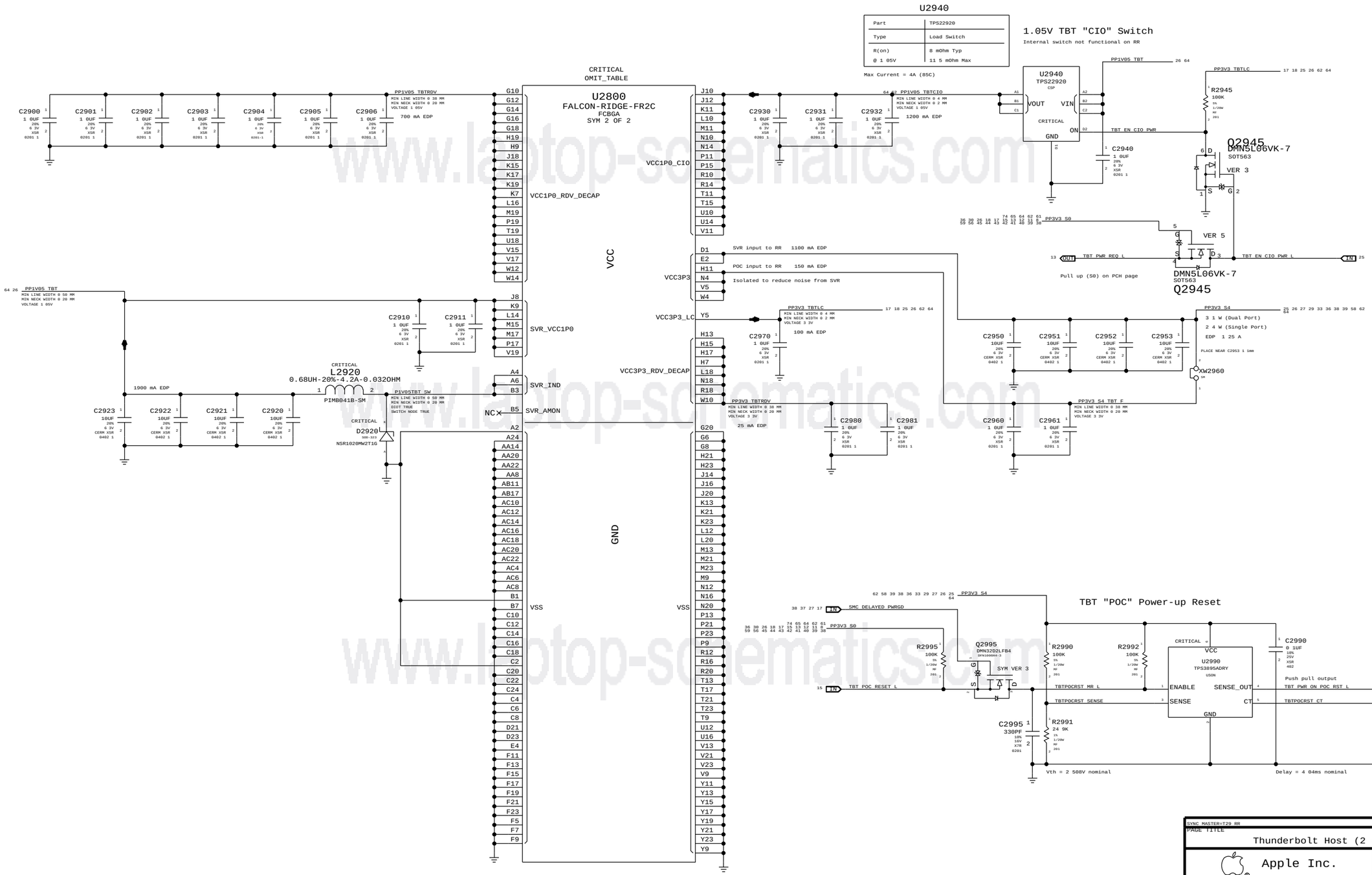

Page Notes

Power aliases required by this page
- =PPVIN SW TBTBST (8 13V Boost Input)
- =PP15V TBT REG (15V Boost Output)

Signal aliases required by this page
(NONE)

BOM options provided by this page
(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): 1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

62 56 50 49 42 41 64 PPBUS_G3H
8-13V Input
Changes required
for 2S.

CRITICAL Q3080 SI8409DB BGA

PPVIN_S4SW_TBTBST_FET
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
Voltage not specified here
add property on another page

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_L

Q3005 DMN32D2LFB4 SYM VER 2
28 25 IN TBT_A_HV_EN

C3090 10UF 20% 25V X5R CERM 0603
C3091 10UF 20% 25V X5R CERM 0603

R3091 200K 1% 1/20W MF 201 <R1>
TBTBST_EN_UVLO

C3081 2.2UF 20% 10V X5R CERM 402
C3092 2.2UF 20% 10V X5R CERM 402
C3087 47PF 5% 25V C0G 0201
TBTBST_VC_RC
C3093 3300PF 10% 10V X7R CERM 0201
R3093 10K 1% 1/20W MF 201
R3094 41.2K 1% 1/20W MF 201
R3092 73.2K 1% 1/20W MF 201 <R2>
C3082 2.2UF 20% 10V X5R CERM 402
C3094 0.33UF 10% 6.3V CERM X5R 402

TBTBST_INTVCC
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm
TBTBST_VC
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm
TBTBST_RT
TBTBST_SS
GND_TBTBST_SGND
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

CRITICAL U3090 LT3957 QFN
25 EN/UVLO
28 INTVCC
30 VC
33 RT
32 SS
34 SYNC
27 VIN
8 9 20 21 38 SW
6 SNS1
3 SNS2
1 2 16 35 36 NC
31 FBX
4 23 24 37 SGND
12 13 14 15 16 17 GND

SGND shorted to GND inside package no XW necessary

CRITICAL L3095 6.8UH-4.0A PIMB062D SM

TBTBST_BOOST
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
SWITCH NODE=TRUE
DIDT=TRUE
TBTBST_SNS1
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm
TBTBST_SNS2
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm

R3089 0 5% 1/20W MF 0201
XW3095 SM PLACE NEAR=C3095 1 2 mm
TBTBST_VSNS
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm

R3090 49.9K 1% 1/10W MF LF 402
C3088 22PF 5% 50V CER C0G 0402
TBTBST_VSNS_RC
R3095 133K 1% 1/10W MF LF 402 <Ra>
TBTBST_FBX
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm
NO STUFF C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/10W MF LF 402 <Rb>

Vout = 1.6V * (1 + Ra / Rb)

CRITICAL D3095 POWERDI 123 DFLS230L

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

C3095 10UF 20% 25V X5R CERM 0603
C3097 10UF 20% 25V X5R CERM 0603
C3096 10UF 20% 25V X5R CERM 0603
C3098 10UF 20% 25V X5R CERM 0603
C3084 10UF 20% 25V X5R CERM 0603
C3309A 10UF 20% 25V X5R CERM 0603
C3099 0.001UF 10% 50V X7R CERM 0402
C3085 10UF 20% 25V X5R CERM 0603
C3309B 10UF 20% 25V X5R CERM 0603

Q3088 DMN5L06VK-7 SOT563 VER 3
R3088 330K 5% 1/20W MF 201
Max Vgs 10V
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201
Q3088 DMN5L06VK-7 SOT563 VER 3
SMC_DELAYED_PWRGD
IN 17 26 37 38

BATLOW# Isolation

Q3000 DMN32D2LFB4 SYM VER 3
PP3V3_S4 25 26 29 33 36 38 39 58 62 64
Pull up on RR page
37 13 IN PM_BATLOW_L
TBT_BATLOW_L OUT 25 27
TBT_BATLOW_L 25 27
MAKE BASE TRUE

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012
PAGE TITLE: TBT Power Support
Apple Inc.
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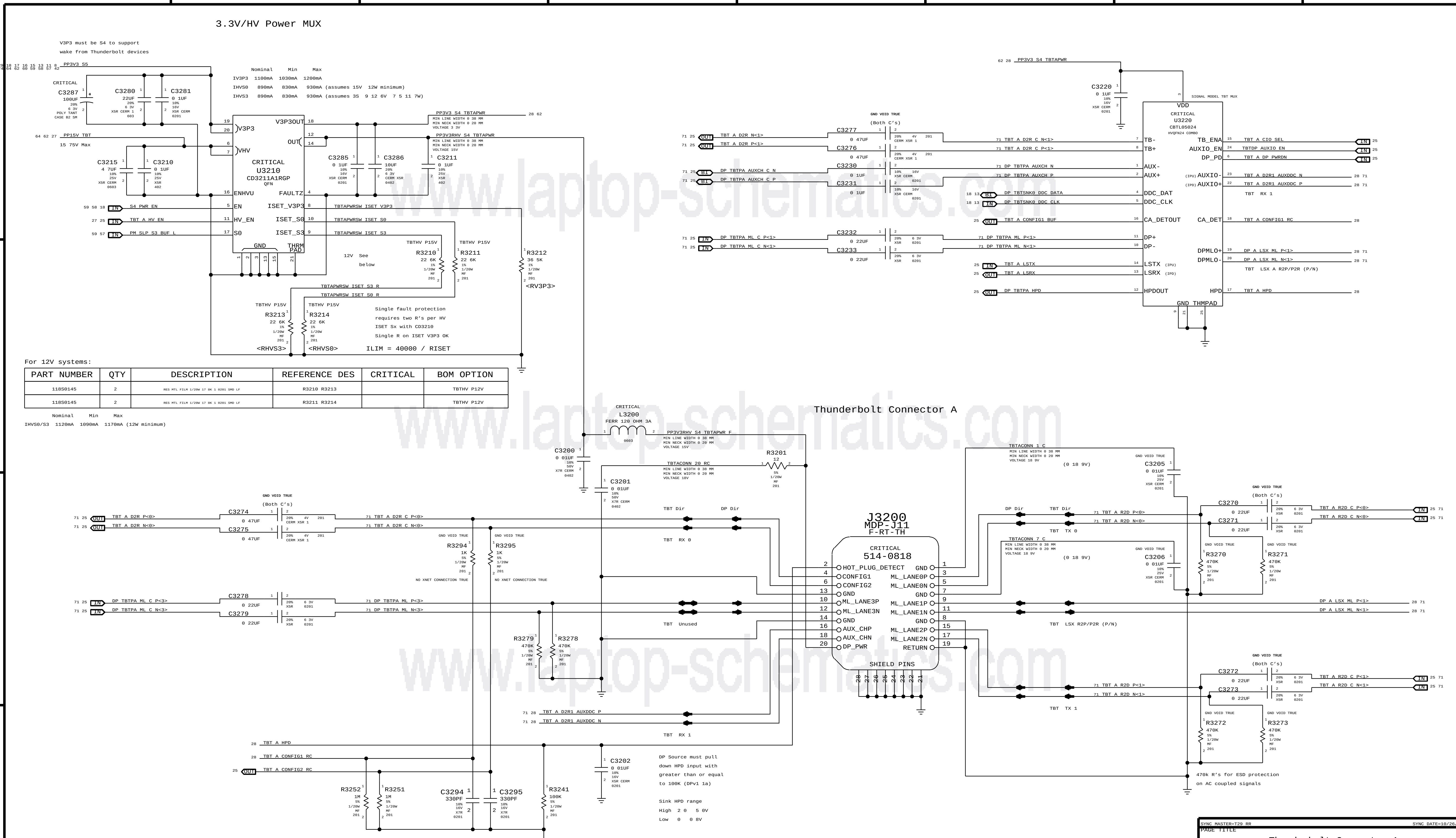
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S 9 12 6V 7 5 11 7W)



PP3V3 S5
CRITICAL
C3287
C3280
C3281
PP15V TBT
15 75V Max
C3215
C3210
CRITICAL
U3210
CD3211A1RGP
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
C3285
C3286
C3211
PP3V3 S4 TBTAPWR
PP3V3RHV S4 TBTAPWR
S4 PWR EN
TBT A HV EN
PM SLP S3 BUF L
TBTAPWRSW ISET V3P3
TBTAPWRSW ISET S0
TBTAPWRSW ISET S3
TBTHV P15V
R3210
R3211
R3212
12V See below
<RV3P3>
R3213
R3214
<RHVS3>
<RHVS0>
Single fault protection
requires two R's per HV
ISET Sx with CD3210
Single R on ISET V3P3 OK
ILIM = 40000 / RISET
PP3V3 S4 TBTAPWR
C3220
VDD
CRITICAL
U3220
CBTL05024
HVQFN24 COMBO
SIGNAL MODEL TBT MUX
GND VOID TRUE
(Both C's)
C3277
C3276
C3230
C3231
C3232
C3233
TBT A D2R N<1>
TBT A D2R P<1>
DP TBTPA AUXCH C N
DP TBTPA AUXCH C P
DP TBTPA ML C P<1>
DP TBTPA ML C N<1>
DP TBTSNK0 DDC DATA
DP TBTSNK0 DDC CLK
TBT A CONFIG1 BUF
TBT A LSTX
TBT A LSRX
DP TBTPA HPD
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND THMPAD
TBT A CIO SEL
TBTDP AUXIO EN
TBT A DP PWRDN
TBT A D2R1 AUXDDC N
TBT A D2R1 AUXDDC P
TBT RX 1
TBT A CONFIG1 RC
DP A LSX ML P<1>
DP A LSX ML N<1>
TBT LSX A R2P/P2R (P/N)
TBT A HPD
Thunderbolt Connector A
CRITICAL
L3200
FERR 120 OHM 3A
PP3V3RHV S4 TBTAPWR F
C3200
R3201
C3201
TBTACONN 20 RC
TBTACONN 1 C
TBTACONN 7 C
C3205
C3206
(0 18 9V)
C3274
C3275
TBT A D2R P<0>
TBT A D2R N<0>
TBT A D2R C P<0>
TBT A D2R C N<0>
TBT Dir
DP Dir
TBT RX 0
R3294
R3295
NO XNET CONNECTION TRUE
C3278
C3279
DP TBTPA ML C P<3>
DP TBTPA ML C N<3>
DP TBTPA ML P<3>
DP TBTPA ML N<3>
TBT Unused
R3279
R3278
J3200
MDP-J11
F-RT-TH
CRITICAL
514-0818
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
TBT A R2D P<0>
TBT A R2D N<0>
TBT TX 0
C3270
C3271
TBT A R2D C P<0>
TBT A R2D C N<0>
R3270
R3271
DP A LSX ML P<1>
DP A LSX ML N<1>
TBT LSX R2P/P2R (P/N)
C3272
C3273
TBT A R2D P<1>
TBT A R2D N<1>
TBT A R2D C P<1>
TBT A R2D C N<1>
TBT TX 1
R3272
R3273
470k R's for ESD protection
on AC coupled signals
TBT A D2R1 AUXDDC P
TBT A D2R1 AUXDDC N
TBT RX 1
TBT A HPD
TBT A CONFIG1 RC
TBT A CONFIG2 RC
R3252
R3251
C3294
C3295
R3241
C3202
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1 1a)
Sink HPD range
High 2 0 5 0V
Low 0 0 8V

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES MTL FILM 1/20W 17 8K 1 0201 SMD LF	R3210 R3213		TBTHV P12V
118S0145	2	RES MTL FILM 1/20W 17 8K 1 0201 SMD LF	R3211 R3214		TBTHV P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

SYNC MASTER=T29 RR SYNC DATE=10/26/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
37 38 39 41 64

PP3V3_WLAN_R
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
Max Current = 2A (85C)

U3550
TPS22924
CSP
A1 VOUT
B1 CRITICAL
VIN A2
ON B2
GND C2
C1

PP3V3_S5
8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 64 74

SMC_WIFI_PWR_EN
IN 29 37 39

C3550
1.0UF
20%
6.3V
X5R
0201 1

C3521
0.1UF
10%
6.3V
CERM X5R
0201
BYPASS=J3501 5mm

514S0335
CRITICAL
J3501
SSD-K99
F RT SH1

AIRPORT

		WIFI_EVENT_L	OUT 37 38 64
69 64 PCIE_AP_R2D_N	C3531 0.1UF 10% 16V X5R CERM 0201	PCIE_AP_R2D_C_N	IN 14 69
69 64 PCIE_AP_R2D_P	C3530 0.1UF 10% 16V X5R CERM 0201	PCIE_AP_R2D_C_P	IN 14 69
		PCIE_CLK100M_AP_N	IN 12 64 69
		PCIE_CLK100M_AP_P	IN 12 64 69
		PCIE_AP_D2R_P	OUT 14 64 69
		PCIE_AP_D2R_N	OUT 14 64 69

PP3V3_S4
25 26 27 29 33 36 38 39 58 62 64

C3532
0.1UF
10%
6.3V
CERM X5R
0201
BYPASS=J3501 1 5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

PP3V3_S5
8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 64 74

C3540
0.1UF
10%
6.3V
CERM X5R
0201

APCLKRQ:ISOL
R3553
100K
5%
1/20W
MF
201

R3554
232K
1%
1/20W
MF
201

P3V3WLAN_VMON

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
*DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R3558
0
5%
1/20W
MF
0201

64 AP_RESET_CONN_L
AP_RESET_CONN_R_L
AP_RESET_L
IN 15

SMC_WIFI_PWR_EN
IN 29 37 39

64 AP_CLKREQ_Q_L
AP_CLKREQ_R_L

R3555
100K
1%
1/20W
MF
201

APCLKRQ:ISOL
R3556
0
5%
1/20W
MF
0201

APCLKRQ:BIDIR
R3557
0
5%
1/20W
MF
0201

AP_CLKREQ_L
BI 12

NOSTUFF
R3559
0
5%
1/20W
MF
0201

PCIe Wake Muxing

60 59 58 13 11 10 PP3V3_S5 17 16 15 57 42 33 74 64 62

R3561
100K
5%
1/20W
MF
201

C3560
0.1UF
10%
6.3V
CERM X5R
0201

U3560
NC7SB3157P6XG
SC70
VER-3
VCC
CRITICAL
GND
S AP_S0IX_WAKE_SEL IN 15
B0 PCIE_WAKE_L OUT 13 31 64
B1 AP_S0IX_WAKE_L OUT 15
A AP_PCIE_WAKE_L

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

NOSTUFF
R3560
0
5%
1/20W
MF
0201

36 33 29 27 26 25 33 58 PP3V3_S4

BLUETOOTH

C3510
0.1UF
10%
6.3V
CERM X5R
0201

U3510
USB3740
DFN
CRITICAL
VDD
DP_2 USB_BT_P BI 14 68
DM_2 USB_BT_N BI 14 68
DP_1 NC
DM_1 BT_WAKE
OE*
S PM_SLP_S4_L IN 13 18 36 37 59
DP
DM
GND

68 64 USB_BT_CONN_P
68 64 USB_BT_CONN_N

SIGNAL_MODEL=BT_MUX

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

NO XNET CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H3
SYM VER 2

SMC_PME_S4_WAKE_L
OUT 36 37 39

R3512
15K
1%
1/20W
MF
201

SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	Wireless Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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PLACE NEAR=J3700 1 3mm
CRITICAL
L3700
FERR-26-OHM-6A
0603
64 62 41 30 PP3V3_S0SW_SSD
64 PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0 6mm
MIN_NECK_WIDTH=0 15mm
VOLTAGE=3 3V
C3701 0.1UF 10% 16V X5R CERM 0201
C3702 0.1UF 10% 16V X5R CERM 0201
PLACE NEAR=L3700 1 1mm
PLACE NEAR=L3700 1 1mm

74 65 64 62 61 36 30 26 18 17 15 13 12 11 8 59 56 45 44 43 42 41 40 39 38 PP3V3_S0

514S0449
CRITICAL
J3700
SSD-GS3
F RT SM
GND VOID
GND VOID

NOSTUFF R3710 100K 5% 1/20W MF 201
NOSTUFF R3700 100K 1% 1/20W MF 201
61 59 56 45 44 43 42 41 40 38 36 30 74 65 64 62 PP3V3_S0

64 15 IN SSD_SR_EN_L
64 SSD_RESET_CONN_L
18 IN SSD_BOOT
SSD_BOOT_R
R3701 0 5% 1/20W MF 0201 NOSTUFF

67 12 IN PCIE_SSD_R2D_C_N<3> C3710 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_P<3> C3711 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_N<2> C3712 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_P<2> C3713 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_N<1> C3714 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_P<1> C3715 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_N<0> C3716 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201
67 12 IN PCIE_SSD_R2D_C_P<0> C3717 0.1UF 10% 16V X5R CERM 0201 GND_VOID=TRUE MF 0201

67 64 PCIE_SSD_R2D_N<3>
67 64 PCIE_SSD_R2D_P<3>
67 64 PCIE_SSD_R2D_N<2>
67 64 PCIE_SSD_R2D_P<2>
67 64 PCIE_SSD_R2D_N<1>
67 64 PCIE_SSD_R2D_P<1>
67 64 PCIE_SSD_R2D_N<0>
67 64 PCIE_SSD_R2D_P<0>
64 SSD_CLKREQ_CONN_L

SSD_PCIE_SEL_L
TP_SSD_DEVSLP
SMC_PWRFAIL_WARN_L
SSD_PWR_EN
SMC PWRFAIL WARN L Signal no connect on X31

PCIE_SSD_D2R_N<3> OUT 12 64 67
PCIE_SSD_D2R_P<3> OUT 12 64 67
PCIE_SSD_D2R_N<2> OUT 12 64 67
PCIE_SSD_D2R_P<2> OUT 12 64 67
PCIE_SSD_D2R_N<1> OUT 12 64 67
PCIE_SSD_D2R_P<1> OUT 12 64 67
PCIE_SSD_D2R_N<0> OUT 12 64 67
PCIE_SSD_D2R_P<0> OUT 12 64 67
PCIE_CLK100M_SSD_N IN 12 64 67
PCIE_CLK100M_SSD_P IN 12 64 67

SMC_OOB1_R2D_CONN_L
SMC_OOB1_D2R_CONN_L

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

PCIe polarity inversion and lane reversal
are only permitted on the device side,
provided the device PHY supports it.

Gumstick3 Connector

OOB Isolation

64 62 41 30 PP3V3_S0SW_SSD
BYPASS=U3710 5 mm
C3718 0.1UF 10% 16V X5R CERM 0201
CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L IN 37
NC
NC

PP3V3_S0
BYPASS=U3711 5 mm
C3719 0.1UF 10% 16V X5R CERM 0201
CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L OUT 37
NC
NC
R3703 100K 1% 1/20W MF 201

R3702 0 5% 1/20W MF 0201
64 30 SSD_PCIE_SEL_L

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD 30 41 62 64
PP3V42_G3H 17 35 36 37 38 40 46 49 50 59 61 62 64 65
R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
C3740 0.1UF 10% 6.3V CERM X5R 0201
CRITICAL
U3740
SLG4AP016V
TDFN
VDD
P3V3SSD_VMON
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
SSD_RESET_L IN 15
SSD_PWR_EN IN 15 30 58 59 64
SSD_CLKREQ_L OUT 12
R3742 100K 1% 1/20W MF 201

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013
PAGE TITLE: SSD Connector
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE

MIPI_AGND
DDR_VDDIO
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
XTAL_AVSS
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_0
SR_VLXD_0
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDD018
XTAL_AVDD1P2

PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V8_CAM
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_XTALPCIEVDD
GND_CAM_PVSSC
GND_CAM_PVSSD
GND_CAM_PVSSD
PP3V3_S3RS0_CAMERA
(=PP3V3_S3RS0_CAMERA)
L3906 22NH 0402
L3902 1.0UH-1.6A-55MOHM 1008
L3903 220-OHM-1.4A 0603
L3904 220-OHM-1.4A 0603
L3901 1.0UH-1.6A-55MOHM 1008
XW3900 SM
XW3901 SM
C3900 0.1UF 10% 6.3V CERM X5R 0201
C3921 1.0UF 20% 6.3V X5R 0201 1
C3922 0.1UF 10% 6.3V CERM X5R 0201
C3923 1.0UF 20% 6.3V X5R 0201 1
C3924 0.1UF 10% 6.3V CERM X5R 0201
C3912 4.7UF 20% 6.3V X5R 402
C3913 4.7UF 20% 6.3V X5R 402
C3927 0.1UF 10% 6.3V CERM X5R 0201
C3930 1.0UF 20% 6.3V X5R 0201 1
C3931 10UF 20% 6.3V CERM X5R 0402 1
C3932 1.0UF 20% 6.3V X5R 0201 1
C3933 10UF 20% 6.3V CERM X5R 0402 1
C3970 0.1UF 10% 6.3V CERM X5R 0201
C3971 1000PF 10% 16V X7R 1 0201
C3972 0.1UF 10% 6.3V CERM X5R 0201
C3973 1000PF 10% 16V X7R 1 0201
C3974 0.1UF 10% 6.3V CERM X5R 0201
C3975 0.1UF 10% 6.3V CERM X5R 0201
C3914 4.7UF 20% 6.3V X5R 402
C3915 4.7UF 20% 6.3V CERM 402
C3919 0.1UF 10% 6.3V CERM X5R 0201
C3918 1000PF 10% 16V X7R 1 0201
C3916 0.1UF 10% 6.3V CERM X5R 0201
C3917 1000PF 10% 16V X7R 1 0201
C3910 0.1UF 10% 6.3V CERM X5R 0201
C3951 0.1UF 10% 6.3V CERM X5R 0201
C3928 4.7UF 20% 6.3V X5R 402
C3938 1000PF 10% 16V X7R 1 0201
C3926 4.7UF 20% 6.3V X5R 402
C3942 4.7UF 20% 6.3V X5R 402
C3940 0.1UF 10% 6.3V CERM X5R 0201
C3934 1000PF 10% 16V X7R 1 0201
C3935 0.1UF 10% 6.3V CERM X5R 0201
C3936 1000PF 10% 16V X7R 1 0201
C3937 0.1UF 10% 6.3V CERM X5R 0201
C3941 2.2UF 20% 6.3V CERM 402 LF
C3939 1UF 10% 10V X5R 402
C3960 0.1UF 10% 6.3V CERM X5R 0201
R3930 100K 5% 1/20W MF 201 NOSTUFF
R3932 100K 5% 1/20W MF 201 NOSTUFF
R3934 100K 5% 1/20W MF 201 NOSTUFF
R3931 330K 5% 1/20W MF 201
R3933 330K 5% 1/20W MF 201
R3935 330K 5% 1/20W MF 201
R3920 100K 5% 1/20W MF 201
R3921 100K 5% 1/20W MF 201
R3936 100K 5% 1/20W MF 201 NOSTUFF
R3937 100K 5% 1/20W MF 201 NOSTUFF
R3913 1K 5% 1/20W MF 201
R3914 1K 5% 1/20W MF 201
R3991 0 5% 1/20W MF 0201 NOSTUFF
R3990 100K 5% 1/20W MF 201
R3901 100K 5% 1/20W MF 201
R3915 100K 5% 1/20W MF 201
R3910 100K 5% 1/20W MF 201 NO STUFF
R3911 100K 5% 1/20W MF 201
R3904 100K 5% 1/20W MF 201
R3906 100K 5% 1/20W MF 201
R3907 100K 5% 1/20W MF 201
R3912 240 1% 1/20W MF 201
R3975 51K 5% 1/20W MF 201
R3976 51K 5% 1/20W MF 201

PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
PLACE_NEAR=U3900.M14 2.54MM
PLACE_NEAR=U3900.K13 4MM
BYPASS=U3900 K13 2.54MM
BYPASS=U3900 F6 2.54MM
BYPASS=U3900 F9 2.54MM
BYPASS=U3900 L9 2.54MM
BYPASS=U3900 J1 2.54MM
BYPASS=U3900 L7 2.54MM
BYPASS=U3900 D6 2.54MM
BYPASS=U3900 D7 2.54MM
BYPASS=U3900 F15 2.54MM
BYPASS=U3900 G15 2.54MM
BYPASS=U3900 7mm 5mm
BYPASS=U3900 3mm 5mm
BYPASS=U3900 3mm 5mm
BYPASS=U3900 5mm

U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE

MEM_CAM_A<0:14>
DDR_AD00:14
MEM_CAM_BA<0:2>
DDR_BA0:2
MEM_CAM_CLK_P/N
DDR_CK_P0/N0
MEM_CAM_DM<0:1>
DDR_DM0/1
MEM_CAM_ZQ_S2
DDR_ZQ
MEM_CAM_CKE
DDR_CKE
MEM_CAM_CS_L
DDR_CS*
MEM_CAM_DQ<0:15>
DDR_DQ00:15
MEM_CAM_DQS_P/N<0:1>
DDR_DQS_P0/N0/P1/N1
MEM_CAM_RAS_L
DDR_RAS*
MEM_CAM_WE_L
DDR_WE*
MEM_CAM_CAS_L
DDR_CAS*
MEM_CAM_RESET_L
DDR_RESET*

U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE

MIPI_CLK_P/N
MIPI_DATA_P/N
MIPI_DP0/DM0
MIPI_DP1/DM1
PCIE_CAMERA_R2D_P/N
PCIE_RDP0/RDN0
PCIE_CLK100M_CAMERA_C_P/N
PCIE_REFCLKP/REFCLKN
PCIE_CAMERA_D2R_C_P/N
PCIE_TDP0/TDN0
PCIE_TESTP/TESTN
CLK25M_CAM_CLKP/CLKN
XTAL_P/XTAL_N
I2C_CAM_SMBDBG_CLK/DAT
I2C_CAM_SCK/SDA
I2C_CLK_DBG/I2C_CLK_SENSOR
I2C_DATA_DBG/I2C_DATA_SENSOR
TP_CAM_JTAG_TCK/TDI/TDO/TMS/TRST_L/SRST_L
JTAG_TCK/TDI/TDO/TMS/TRST*/SRST*
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
PCIE_CLKREQ*/PCIE_RST*/PCIE_WAKE*
CAM_PWR_SEL
CAM_DEBUG_RESET_L
PWR_MODE/RESET*
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
SENSOR_WAKE*/SHUTDOWN*
PCIE_WAKE_L
PU on PCH page
CAM_XTAL_FREQ
PU = 25MHz
CAM_XTAL:YES/NO
CAM_XTAL_SEL
CAM_A1
CAM_JTAG_SRST_L
A1 SILICON BUG
CAM_TEST_MODE
CAM_TEST_OUT

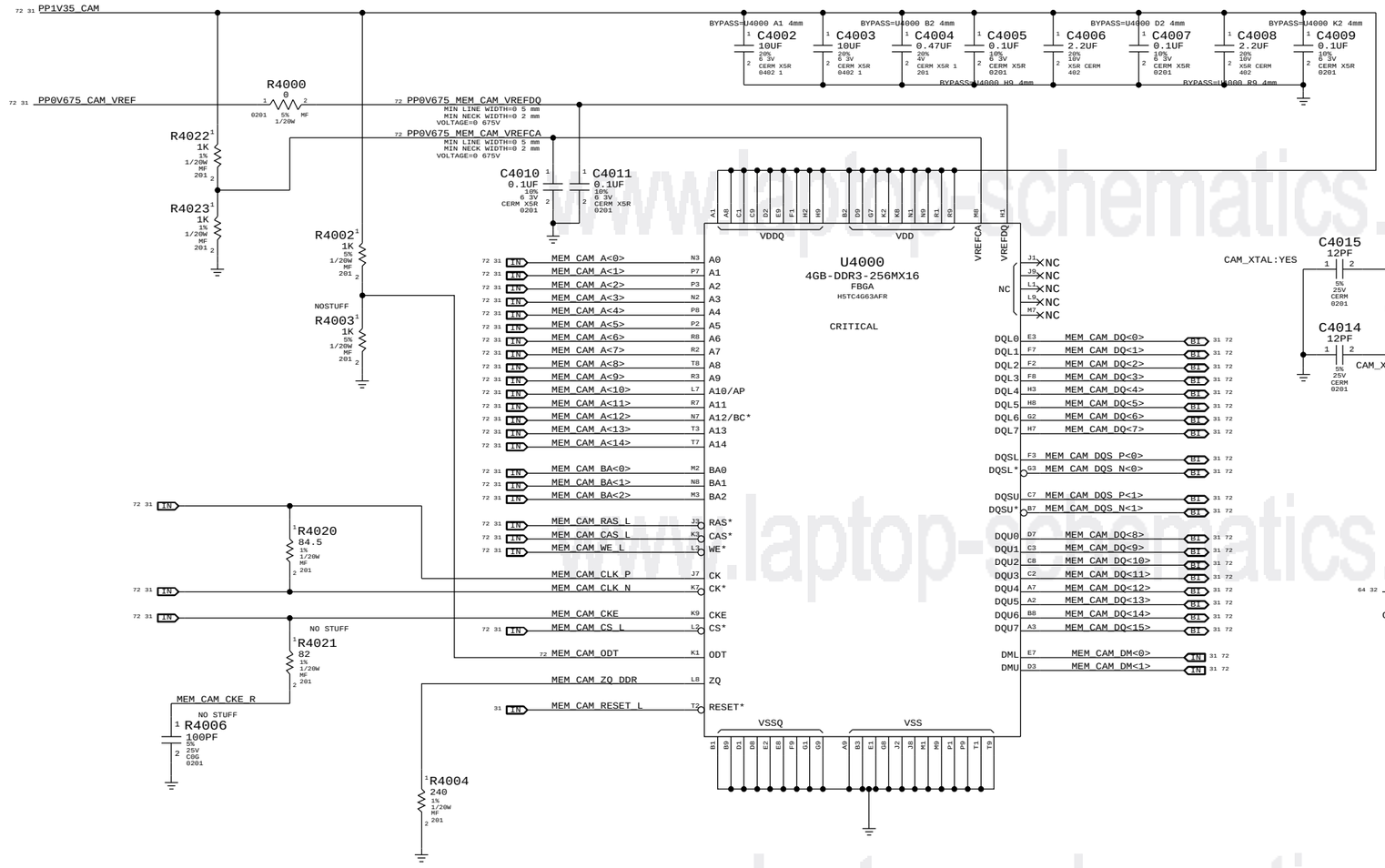
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE

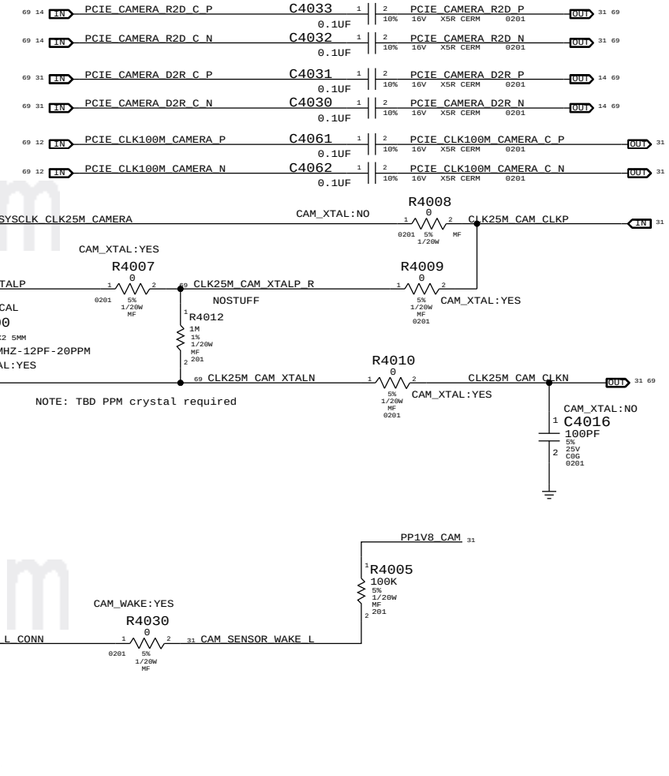
DEBUG_00:16
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK/TDI/TDO/TMS/TRSTN
NC
GPIO_00:07
CAM_RAMCFG0/1/2
CAM_GPIO3
TP_CAM_PLL_BYPASS
UARTCTS/UARTRTS
CAM_UARTCTS/TP_CAM_UARTRTS
UARTRXD/UARTTXD
CAM_UARTRXD/TP_CAM_UARTTXD
TEST_OUT/TEST_MODE
CAM_TEST_OUT/CAM_TEST_MODE
STRAP_XTAL_FREQ/STRAP_XTAL_SEL
CAM_XTAL_FREQ/CAM_XTAL_SEL

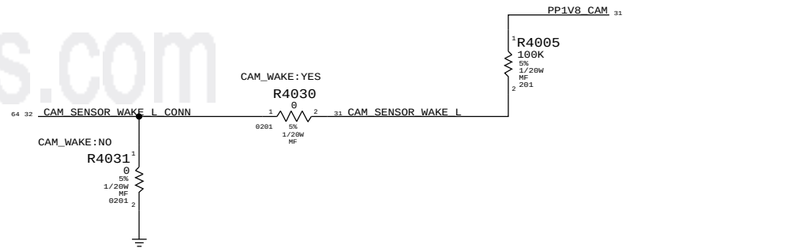
CAM_UARTCTS
CAM_UARTRXD

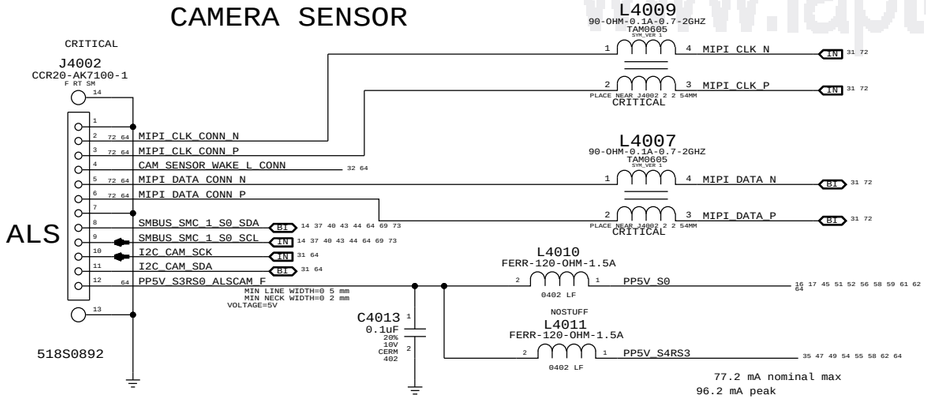
L3901:1 VSENSE_C
L3902:1 VSENSE_D

SYNC_MASTER=J43_MLB1
SYNC_DATE=01/09/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 39 OF 121
SHEET 31 OF 76







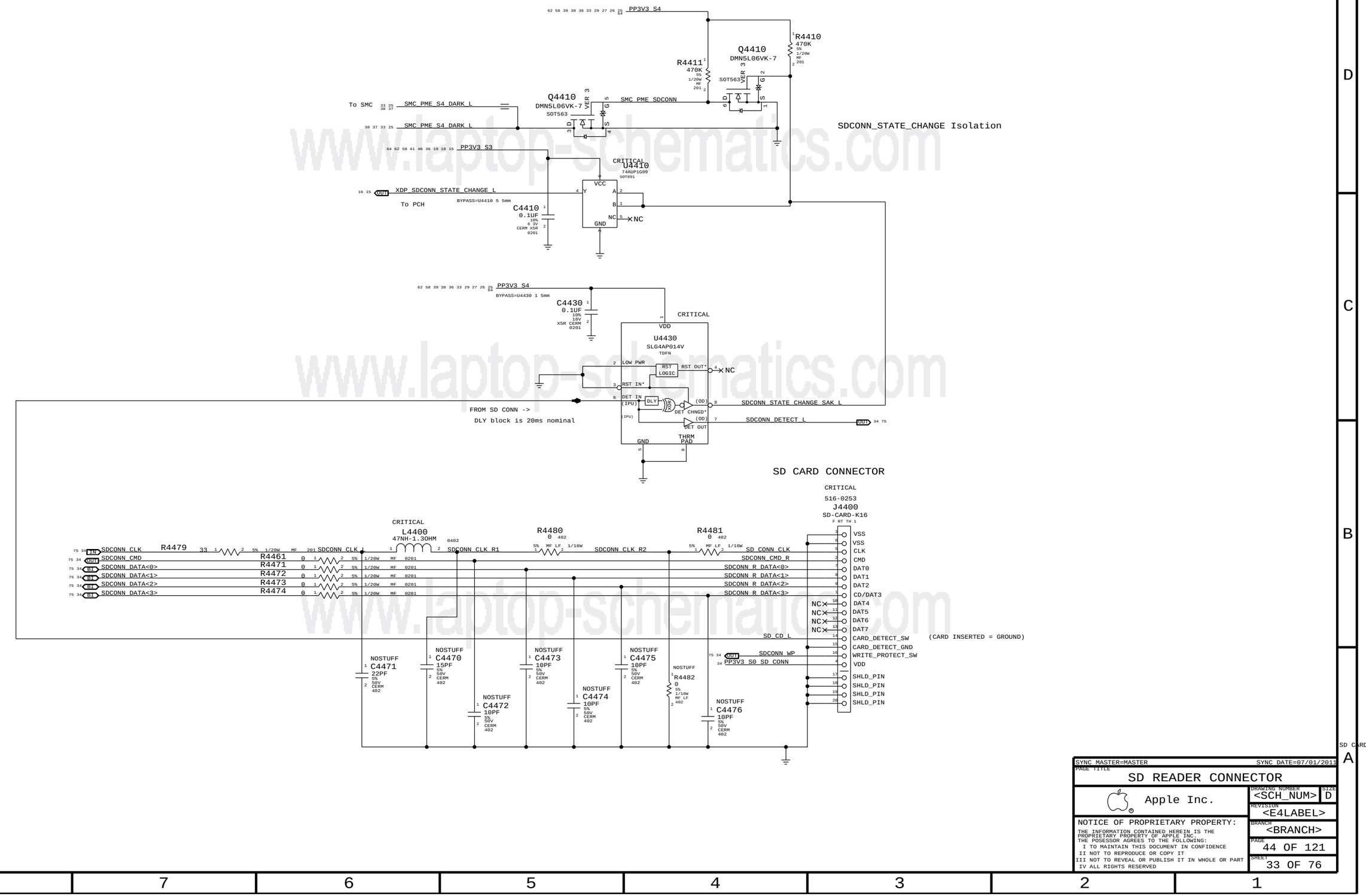


SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 40 OF 121
SHEET: 32 OF 76



SYNC_MASTER=MASTER SYNC_DATE=07/01/2011

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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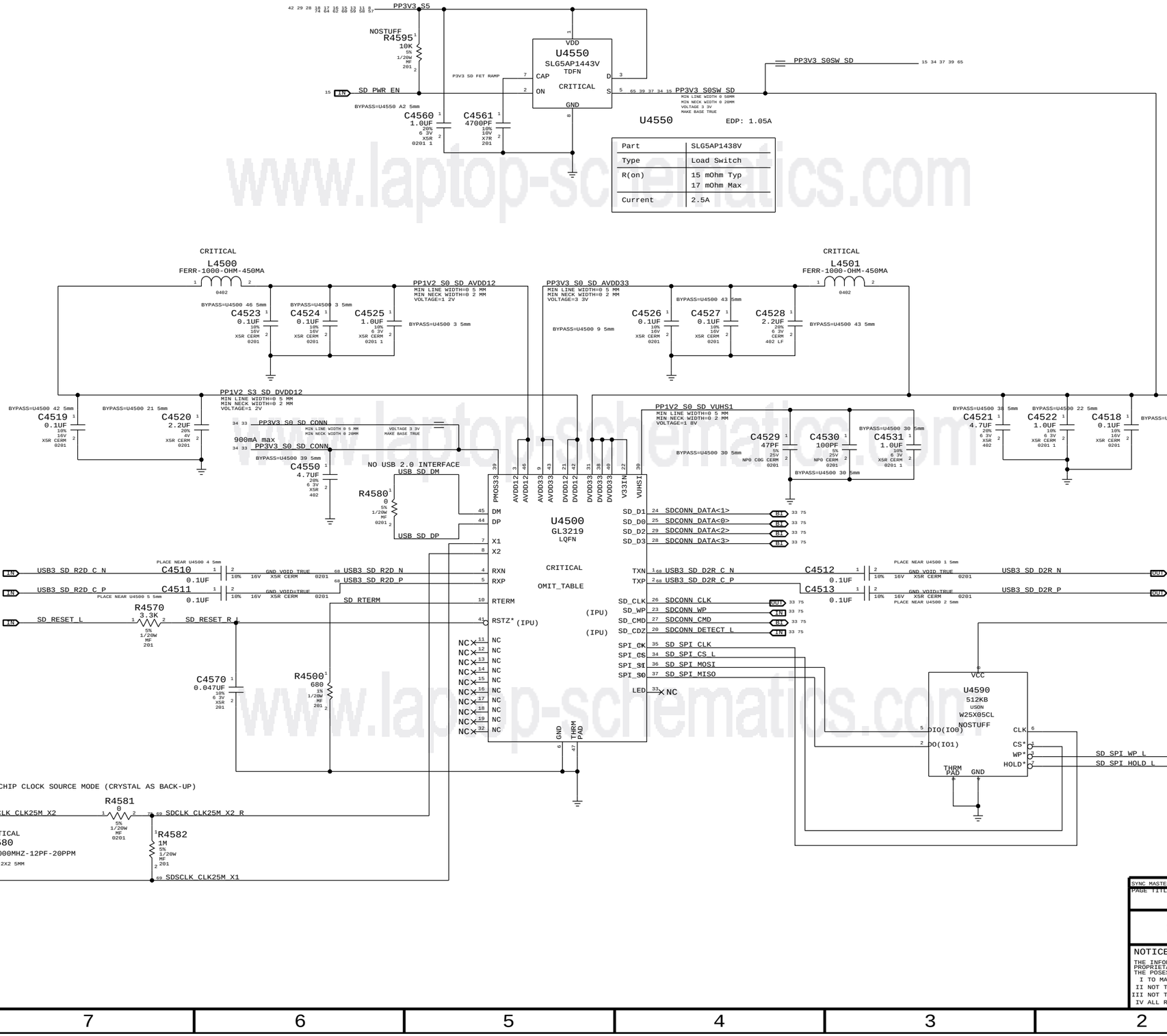
SHEET 33 OF 76

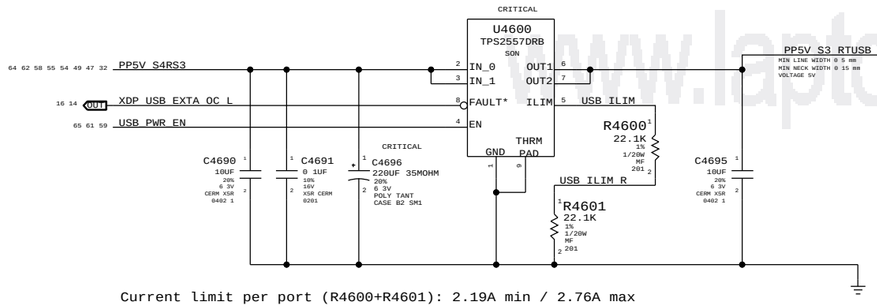
3.3V S3 SD Card Switch



SYNC MASTER=MASTER	SYNC DATE=10/11/2010
PAGE TITLE	SD CONTROLLER (GL3219)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 45 OF 121
	SHEET 34 OF 76

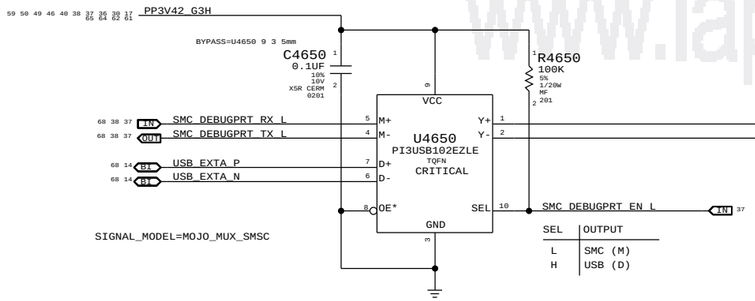
Right USB Port A

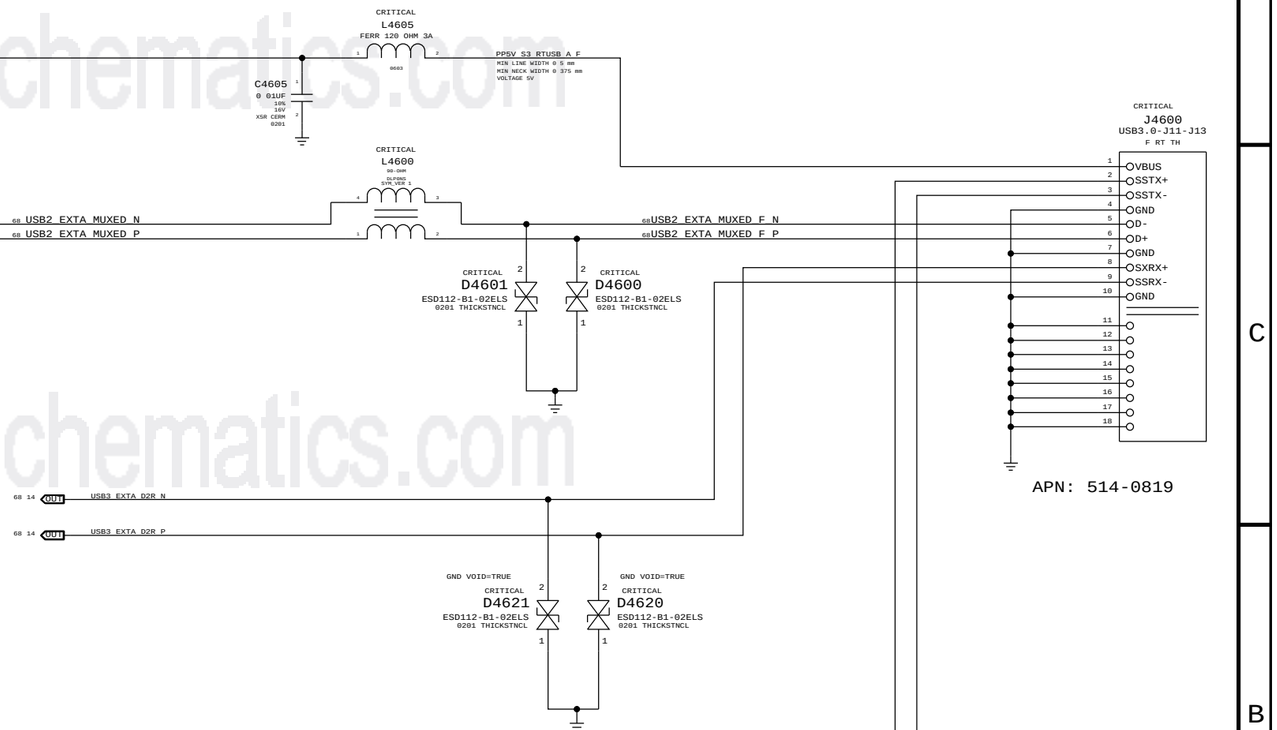
USB Port Power Switch



Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux



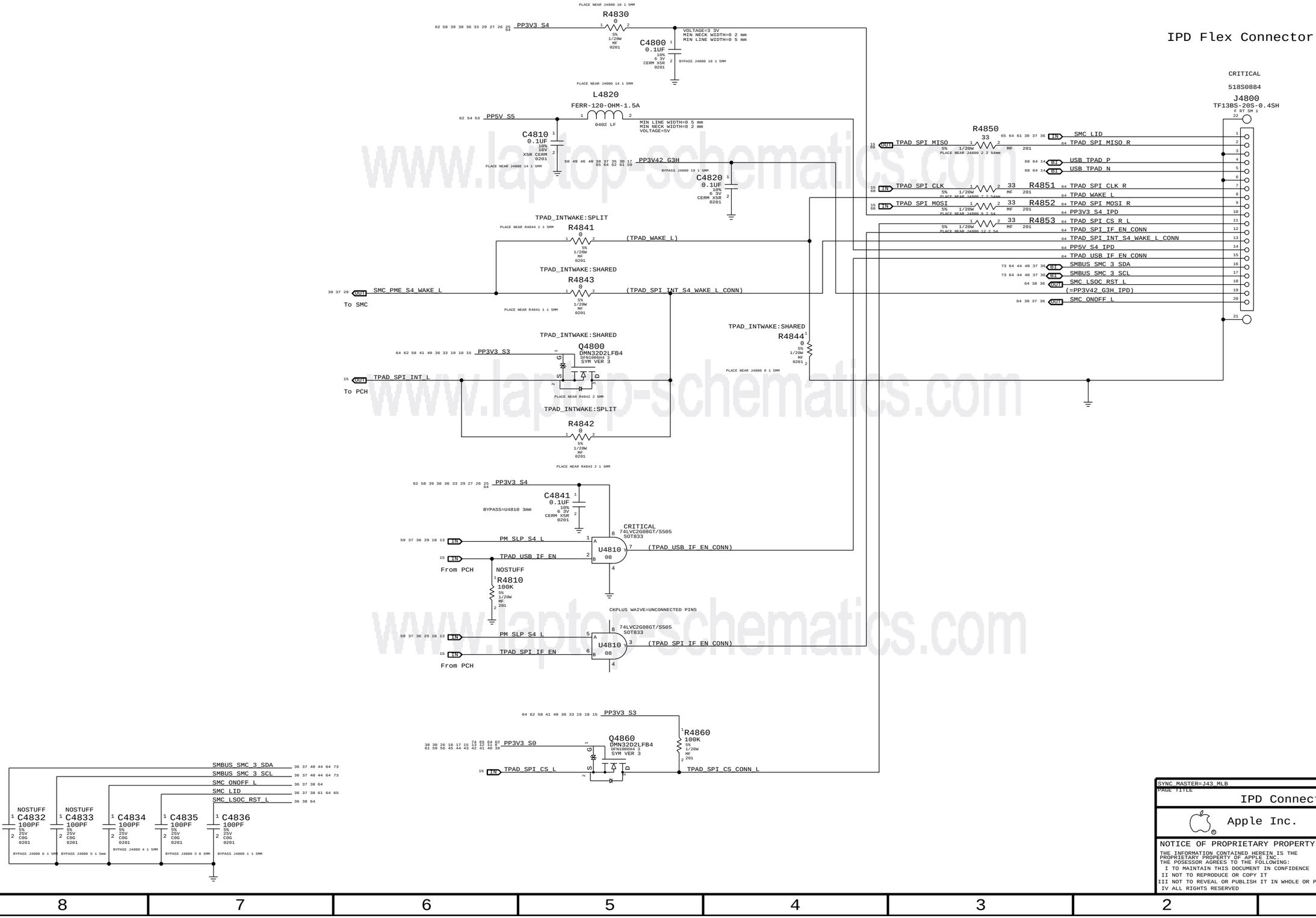


SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

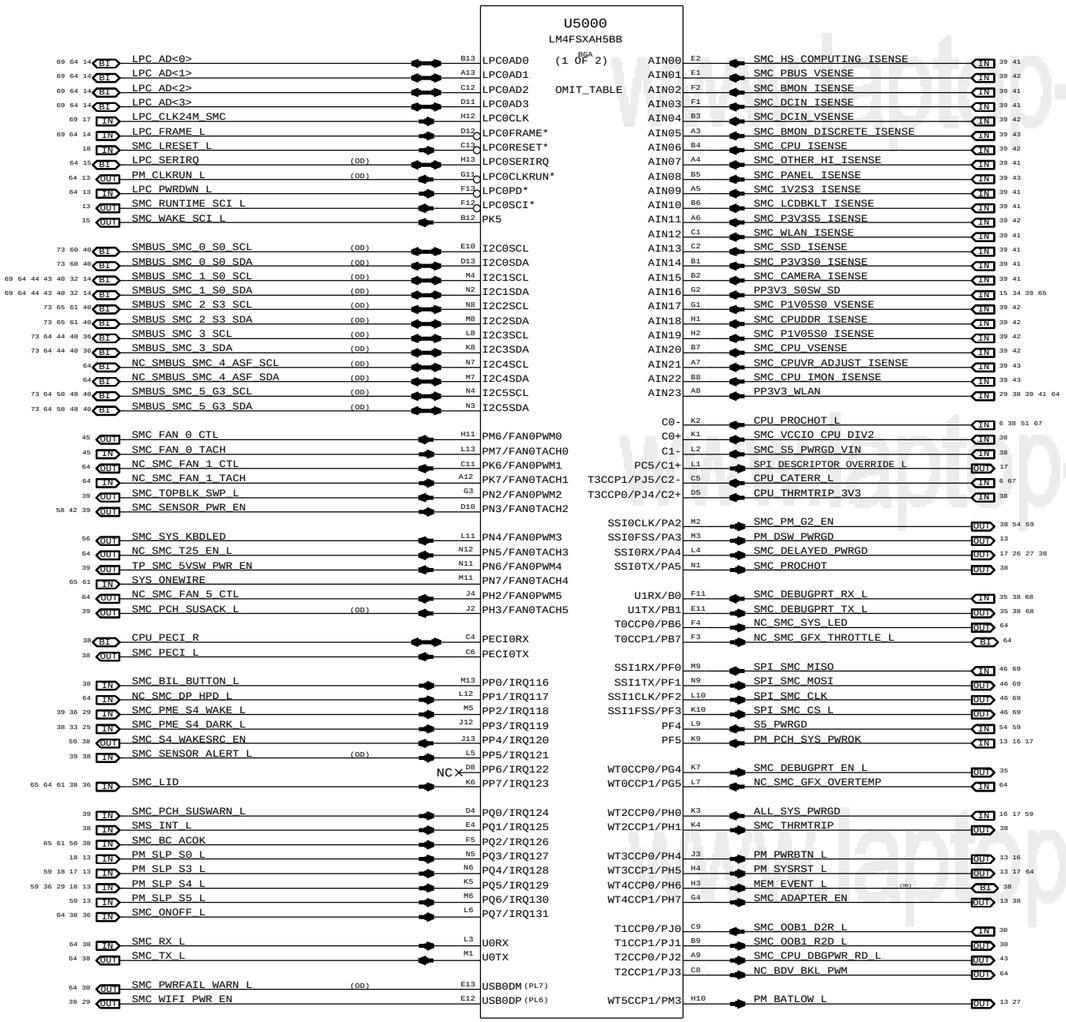
PAGE TITLE: External A USB3 Connector

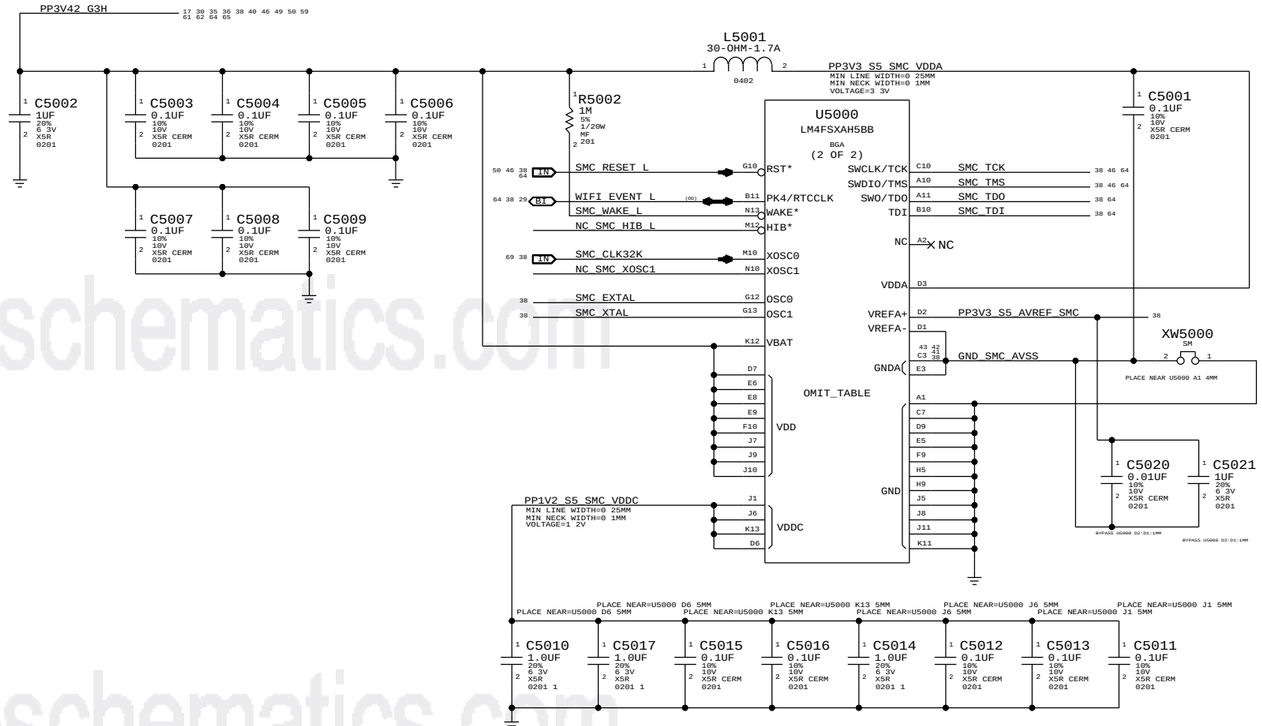
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 121
SHEET: 35 OF 76



SYNC_MASTER=J43_MLB	SYNC_DATE=01/17/2013
PAGE TITLE: IPD Connector	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 48 OF 121
	SHEET: 36 OF 76





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

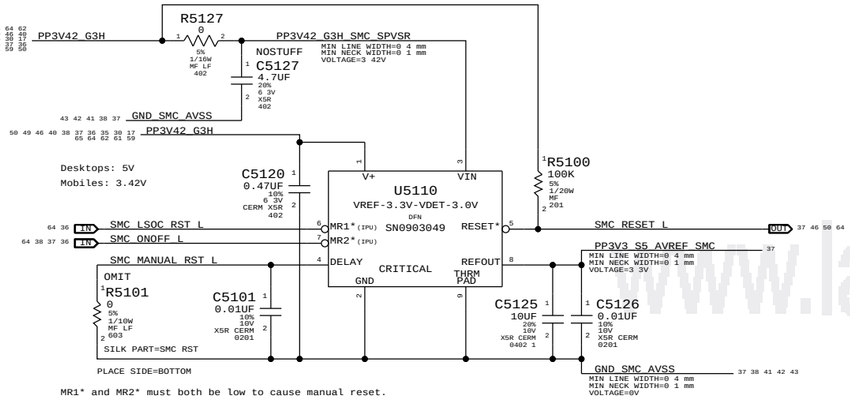
SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
SMC

Apple Inc.

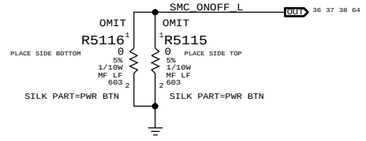
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 50 OF 121
SHEET 37 OF 76

SMC Reset "Button", Supervisor & AVREF Supply



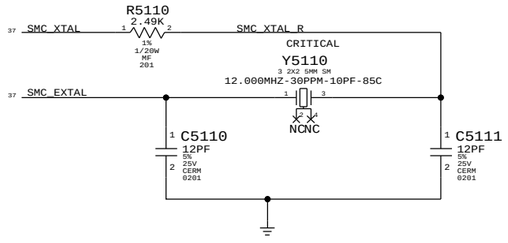
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

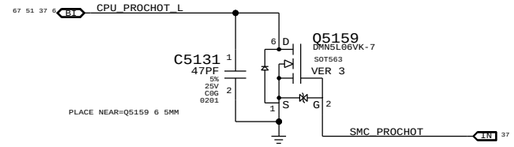
Debug Power "Buttons"

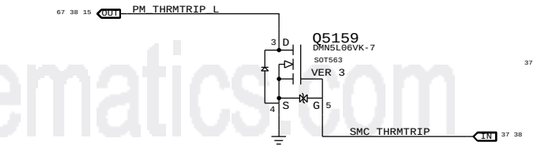


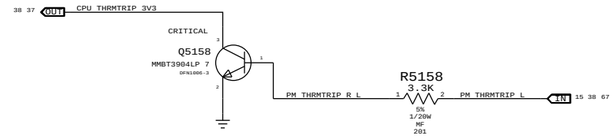
SMC Crystal Circuit

SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

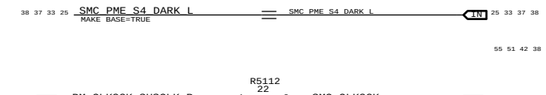


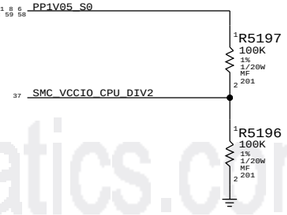




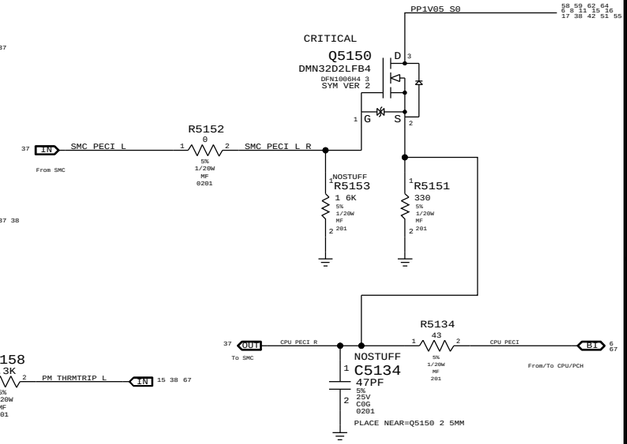


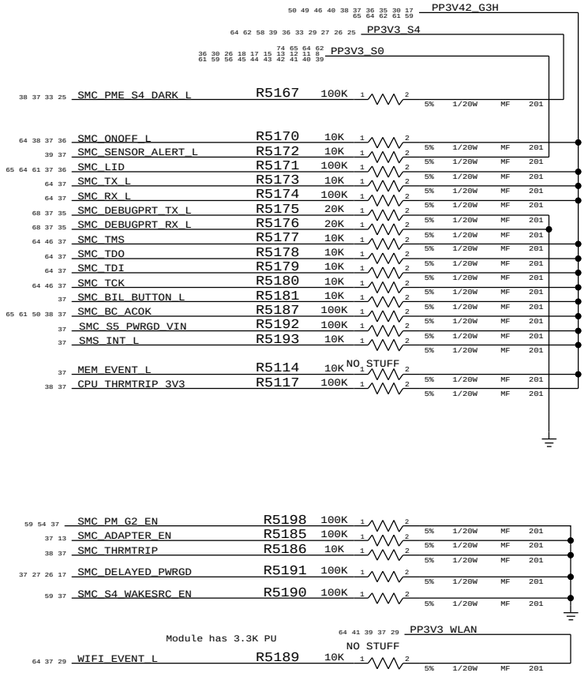
SMC_BC_ACOK — SMC_BC_ACOK
MAKE BASE=TRUE





SMC12 PECI Support





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PAGE TITLE	SMC Shared Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 51 OF 121
	SHEET 38 OF 76

SMC_HS_COMPUTING_ISENSE
SMC_PBUS_VSENSE
SMC_BMON_ISENSE
SMC_DCIN_ISENSE
SMC_DCIN_VSENSE
SMC_BMON_DISCRETE_ISENSE
SMC_CPU_ISENSE
SMC_OTHER_HI_ISENSE
SMC_PANEL_ISENSE
SMC_1V2S3_ISENSE
SMC_LCDBKLT_ISENSE
SMC_P3V3S5_ISENSE
SMC_WLAN_ISENSE
SMC_SSD_ISENSE
SMC_P3V3S0_ISENSE
SMC_CAMERA_ISENSE
PP3V3_S0SW_SD — OUT — SD alias on page 103
SMC_P1V05S0_VSENSE
SMC_CPUDDR_ISENSE
SMC_P1V05S0_ISENSE
SMC_CPU_VSENSE
SMC_CPUVR_ADJUST_ISENSE
SMC_CPU_IMON_ISENSE
PP3V3_WLAN

SMC_SENSOR_PWR_EN
SMC_WIFI_PWR_EN
TP_SMC_5VSW_PWR_EN

R5230 0 — SMC_PCH_SUSWARN_L (IN) — PCH_SUSWARN_L (OUT)
R5231 0 — SMC_PCH_SUSACK_L (OUT) — PCH_SUSACK_L (IN)

Top-Block Swap

PP3V3_S0 — R5296 1K — R5283 1K — SMC_TOPBLK_SWP_L (IN) — PCH_STRP_TOPBLK_SWP_L (OUT)

PP3V3_S4
SMC_WIFI_PWR_EN — R5295 10K NOSTUFF
SMC_SENSOR_PWR_EN — R5294 10K NOSTUFF

PP3V3_S4 — R5282 100K — SMC_PME_S4_WAKE_L (IN) — SMC_PME_S4_WAKE_L (OUT)

SMC_HS_COMP_ALERT_L — R5216 100
PCH_SML1ALERT_L — R5215 100 NOSTUFF
SMC_BMON_COMP_ALERT_L — R5213 100
FINSTACKSNS_ALERT_L — R5210 100
CPUTHMSNS_ALERT_L — R5214 100
CPUBMONSNS_ALERT_L — R5211 100 NOSTUFF
TBTMLBSNS_ALERT_L — R5212 100 — SMC_SENSOR_ALERT_L (OUT)

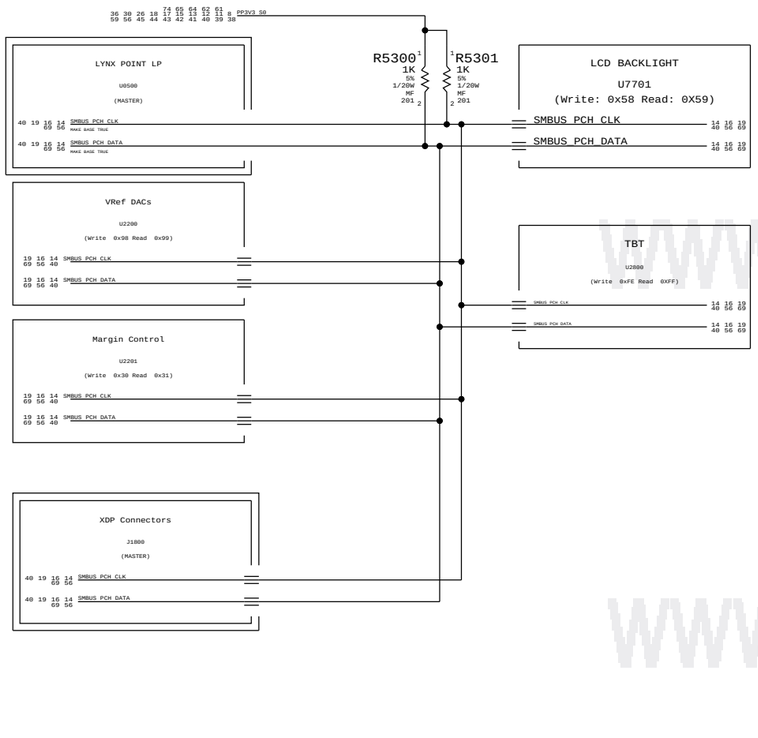
SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: SMC Project Support

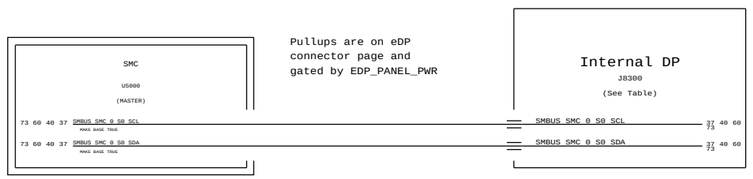
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 52 OF 121
SHEET: 39 OF 76

LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections



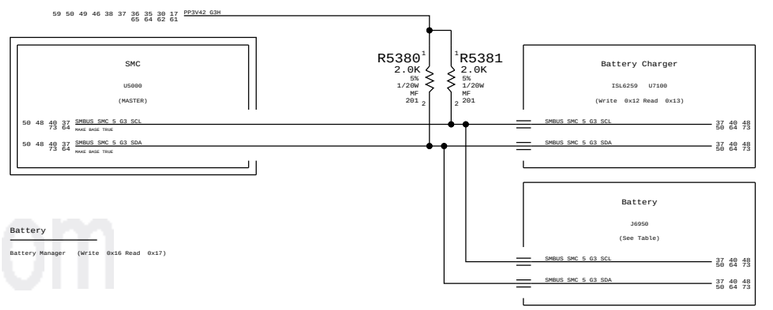
Pullups are on eDP connector page and gated by EDP_PANEL_PWR

(* = Multiple options)

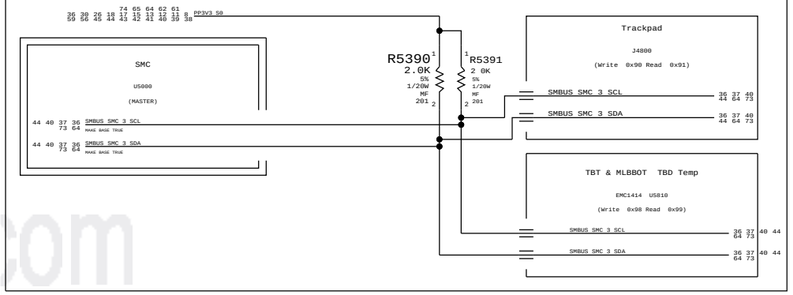
Internal DP

		J43		J41	
		Samsung	LGD	Samsung	LGD AUO
Analogix T con	(Write 0x7B/0x87 Read 0x7C/0xBB)	N Y	*	Y *	
Parade T con	(0x10 0x1F or 0x30 0x3F)	Y N	*	N *	
DVR	(Write 0x4E Read 0x4F)	Y Y	*	Y N	

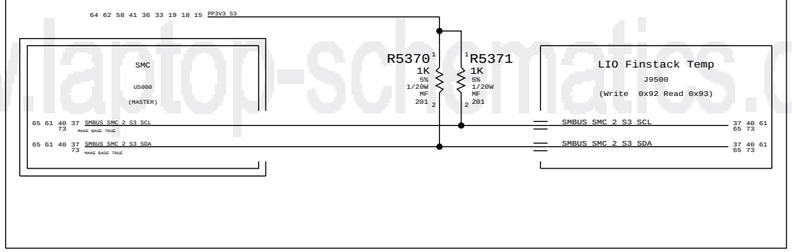
SMC "5" SMBus G3H Connections



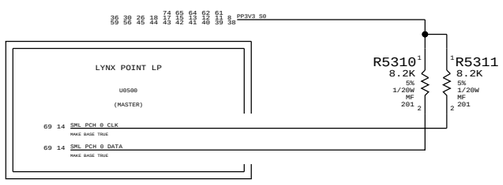
SMC "3" SMBus S0 Connections



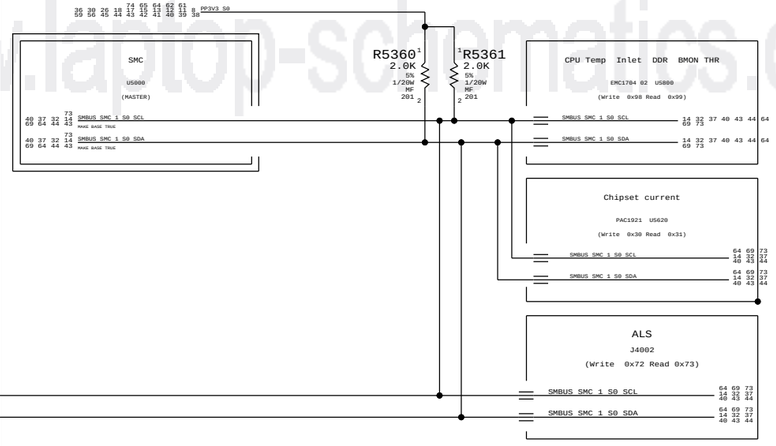
SMC "2" SMBus S3 Connections



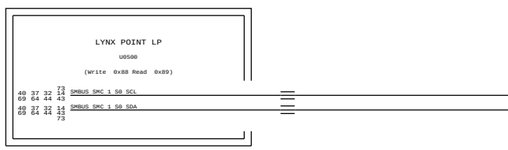
LYNX POINT LP S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to

access PCH

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

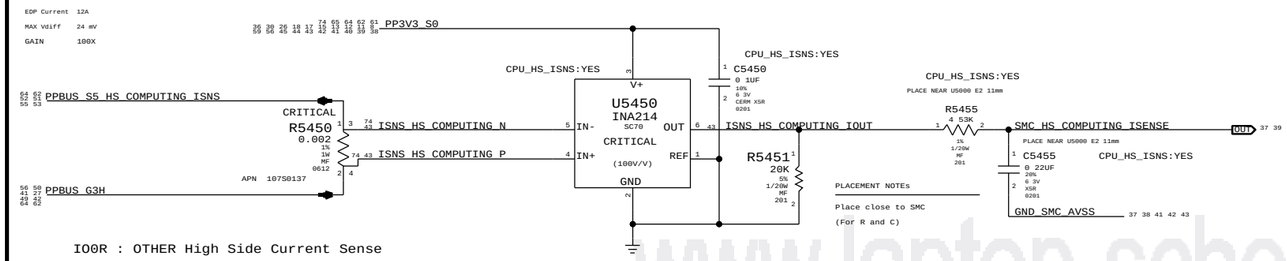
REVISION <E4LABEL>

BRANCH <BRANCH>

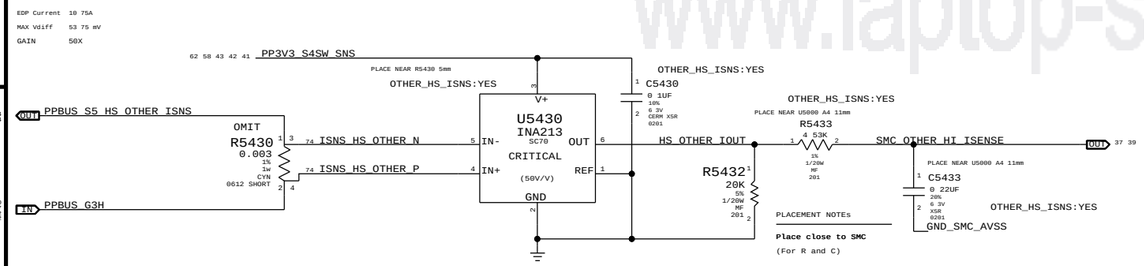
PAGE 53 OF 121

SHEET 40 OF 76

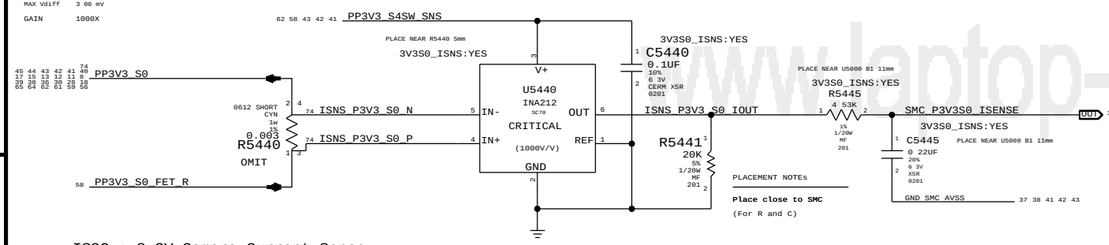
IC0R : COMPUTING High Side Current Sense



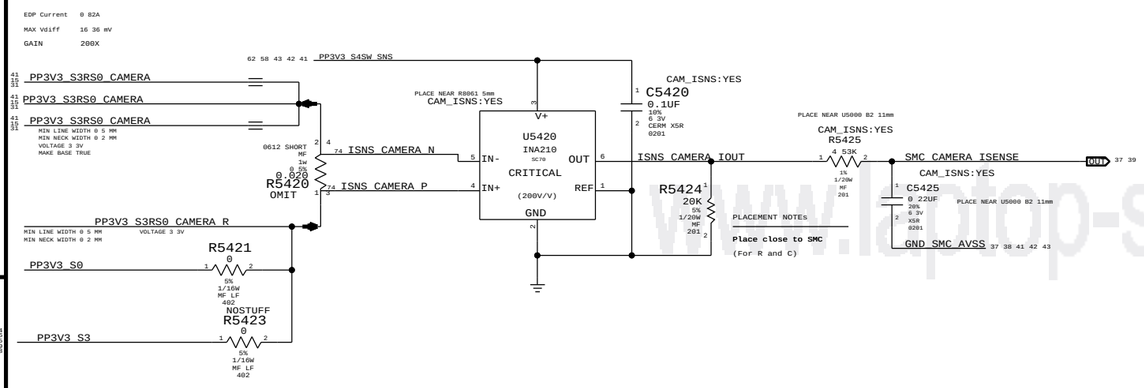
IO0R : OTHER High Side Current Sense



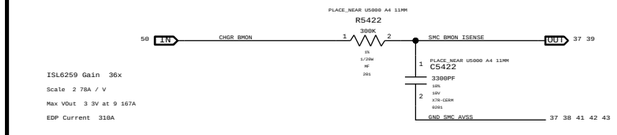
IR0C : 3.3V S0 FET Current Sense



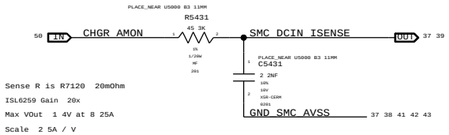
IS2C : 3.3V Camera Current Sense



CHARGER BMON High Side Current Sense

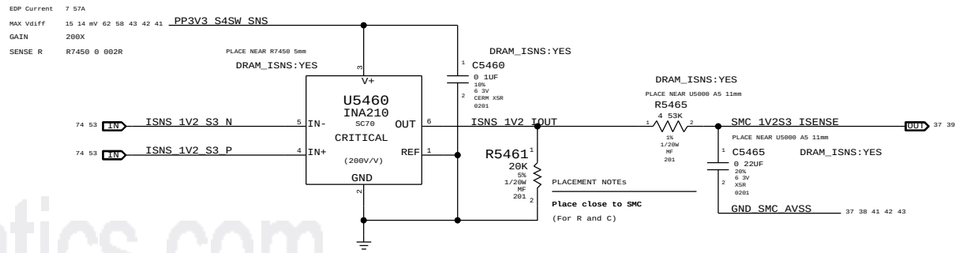


DC-IN (AMON) Current Sense

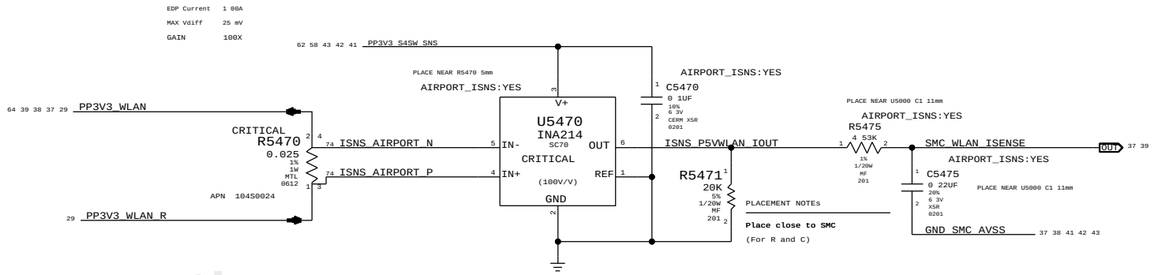


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES SENSE 0 003OHM 1W 4 TERM 1% 0612 TFT	R5480	CRITICAL	

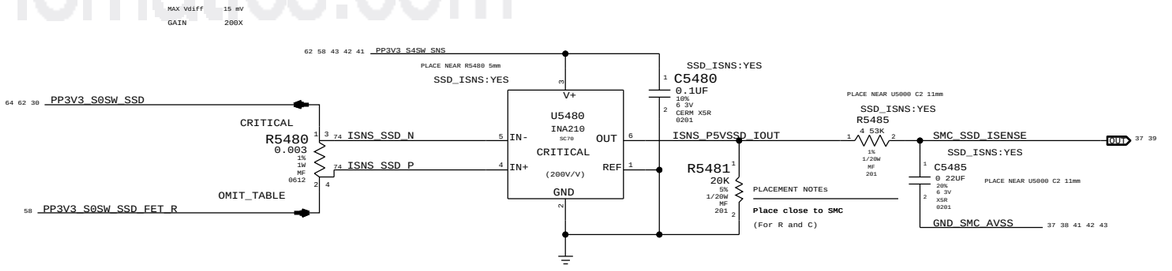
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)



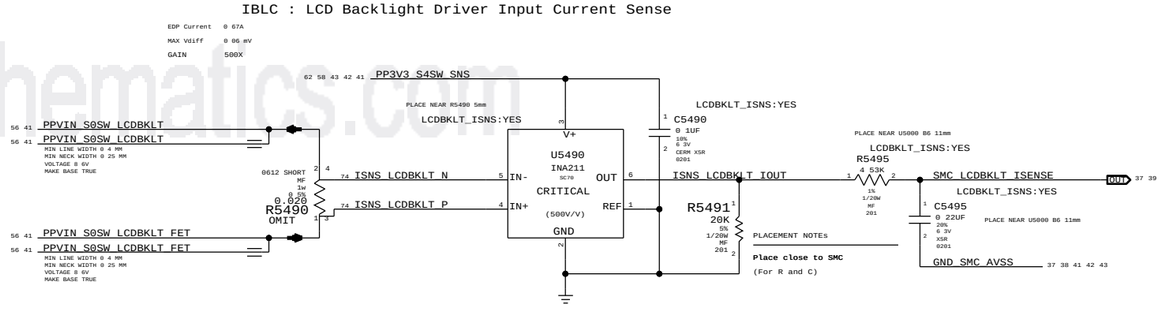
IAPC :AirPort Current Sense



ISDC : SSD Current Sense



IBLC : LCD Backlight Driver Input Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5455		CPU HS ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5465		DRAM ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5475		AIRPORT ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5485		SSD ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5495		LCDBKLT ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5433		OTHER HS ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5425		CAM ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5445		3V3S0 ISNS NO

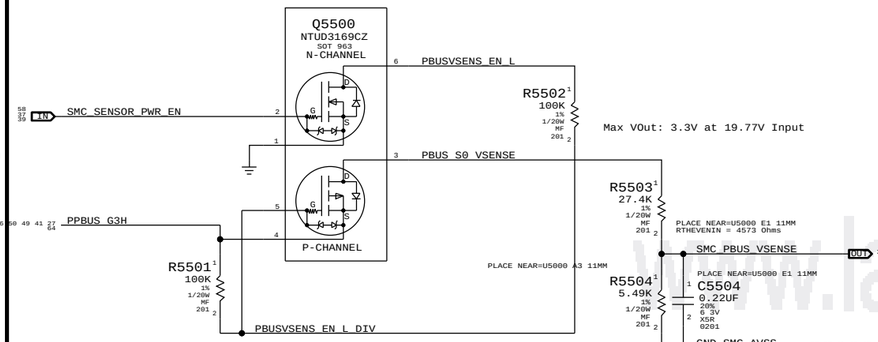
SYNC_MASTER=J41_MLB SYNC_DATE=03/28/2013

PAGE TITLE: High Side Current Sensing

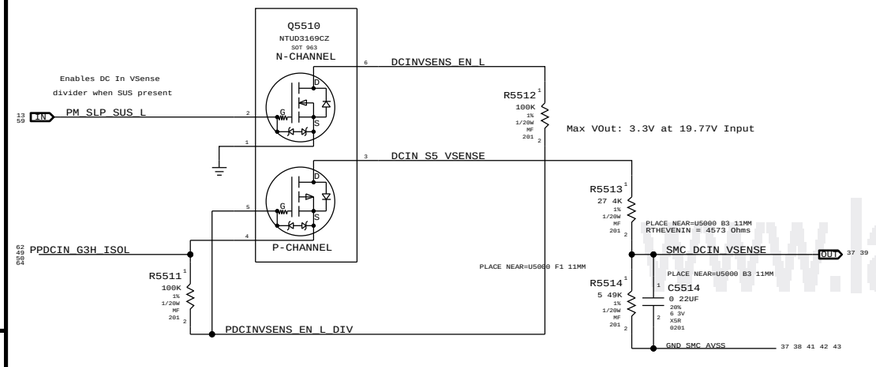
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 121
SHEET: 41 OF 76

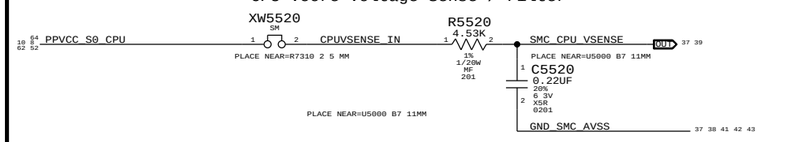
VP0R: PBUS Voltage Sense Enable & Filter



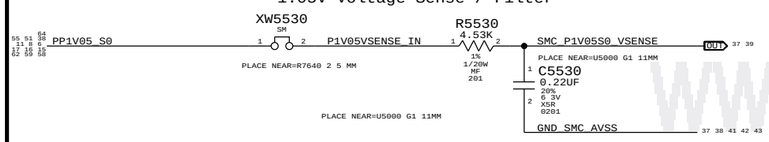
VD0R: DC-In Voltage Sense Enable & Filter



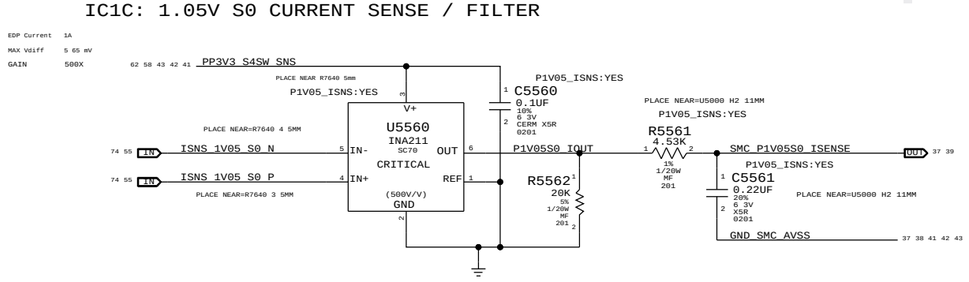
CPU Vcore Voltage Sense / Filter



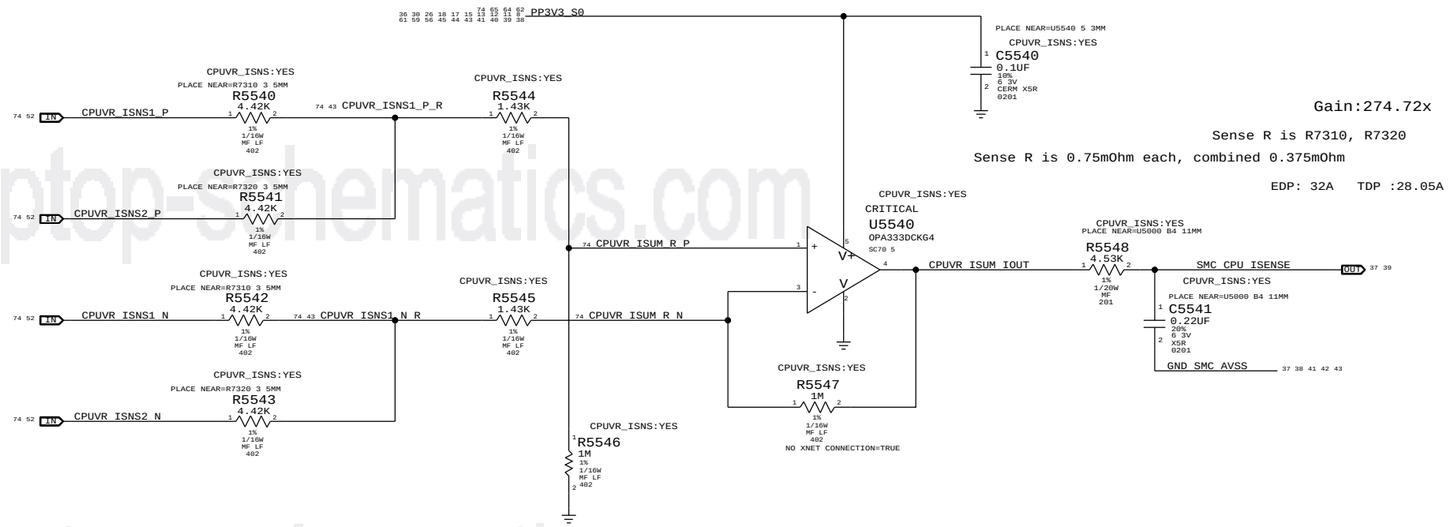
1.05V Voltage Sense / Filter



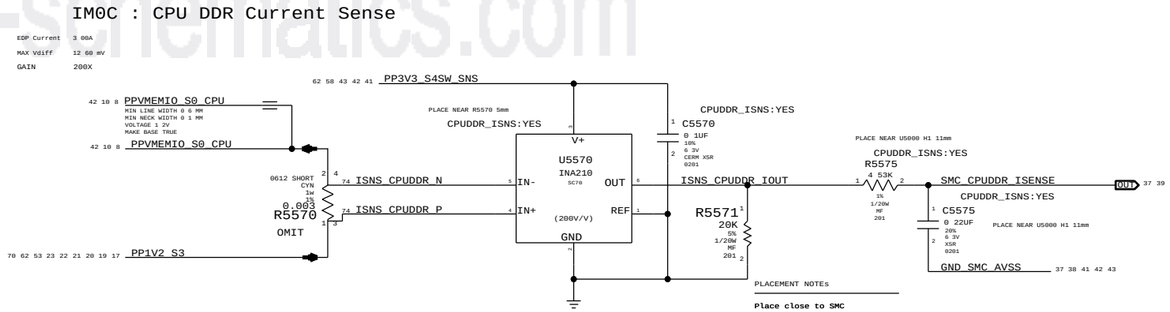
IC1C: 1.05V S0 CURRENT SENSE / FILTER



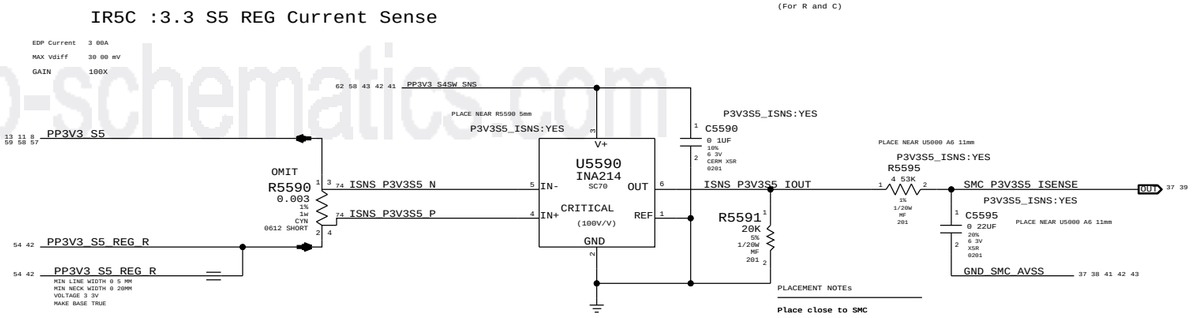
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5541		CPUVR ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5561		P1V05 ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5595		P3V3S5 ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5575		CPUDDR ISNS NO

SYNC_MASTER=J41_MLB SYNC_DATE=03/28/2013

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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ICS3 : Adjustable Gain CPU VR Current

R5821: ADDR - 0x56/0x57 (r/w)

PP3V3_S4SW_SNS

R5620 100 1% 1/16W MF LF 402

PP3V3_SNS_CPUVR_ADJUST_ISNS

C5620 1.0UF 20% 6.3V X5R 0201 1

MIN LINE WIDTH 0.5 mm
MIN NECK WIDTH 0.20 mm
VOLTAGE 3.3V

BYPASS=U5620 1 5 3MM

R5621 4.3K 5% 1/20W MF 201

CPUVRSNS_ADDR_SEL

U5620 PAC1921-1-AIA DFN

ADDR_SEL/GAIN_SEL	6	OUT	4
SENSE+	2	READ*/INT	8
SENSE-	3	SM_CLK/INT_SEL	10
		SM_DATA/OUT_SEL	9
		COMM_SEL	7
GND	5	EPAD	11

VDD

CPUVR_ISNS1_P_R
CPUVR_ISNS1_N_R

PLACE NEAR=U5540 1 5MM

PU: SMBus mode

SMC_CPUVR_ADJUST_ISENSE_R

R5625 0 5% 1/20W MF 0201

PLACE NEAR=U5000 A7 5MM

SMC_CPUVR_ADJUST_ISENSE

C5625 0.22UF 20% 6.3V X5R 0201

NO STUFF

PLACE_NEAR=U5000.A7:5MM

GND_SMC_AVSS

Sense Pins gain stage for U5800 (EMC1704)

PP3V3_S0

R5660 0 5% 1/20W MF 0201

PLACE NEAR=U5660 3 5MM

C5660 0.1UF 10% 6.3V CERM X5R 0201

PLACE NEAR=R7150 5MM

U5660 INA211 SC70 CRITICAL (500V/V)

V+	3		
IN-	5	OUT	6
IN+	4	REF	1
GND	2		

CKPLUS WAIVE=NdifPr badTerm
ISNS_HS_COMPUTING_P
CKPLUS WAIVE=NdifPr badTerm
ISNS_HS_COMPUTING_N

R5663 20K 5% 1/20W MF 201

ISNS_HS_GAIN_OUT

GAIN: 500X

R5665 0 5% 1/20W MF 0201

ISNS_HS_GAIN_OUT_R

NO STUFF

C5665 0.22UF 20% 6.3V X5R 0201

R5666 0 5% 1/20W MF 0201

ISNS_HS_GAIN_P_R — ISNS_HS_GAIN_P — OUT

R5662 1K 1% 1/20W MF 201

ISNS_HS_COMPUTING_P

NO STUFF R5667 0 5% 1/20W MF 0201

R5668 0 5% 1/20W MF 0201

ISNS_HS_GAIN_N_R — ISNS_HS_GAIN_N — OUT

R5661 27K 1% 1/20W MF 201

ISNS_HS_COMPUTING_N

NO STUFF R5669 0 5% 1/20W MF 0201

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

ILDC :LCD Panel Current Sense / Filter

PP3V3_S4SW_SNS

PP3V3_S0SW_LCD
PP3V3_S0SW_LCD

MIN LINE WIDTH 0.3 MM
MIN NECK WIDTH 0.2 MM
VOLTAGE 3.3V
MAKE BASE TRUE

OMIT R5670 0.020 0 5% 1W MF 0612 SHORT

ISNS_PANEL_N
ISNS_PANEL_P

PP3V3_S0SW_LCD_R
PP3V3_S0SW_LCD_R

MIN LINE WIDTH 0.3 MM
MIN NECK WIDTH 0.2 MM
VOLTAGE 3.3V
MAKE BASE TRUE

EDP Current 0.750 A
Max Vdiff 15 mV

PLACE NEAR R5470 5MM
PANEL_ISNS:YES

U5670 INA210 SC70 CRITICAL (200V/V)

V+	3		
IN-	5	OUT	6
IN+	4	REF	1
GND	2		

PANEL_ISNS:YES

C5670 0.1UF 10% 6.3V CERM X5R 0201

ISNS_PANEL_IOUT

PLACE NEAR U5000 C1 11MM

PANEL_ISNS:YES

R5675 4.53K 1% 1/20W MF 201

SMC_PANEL_ISENSE

PANEL_ISNS:YES

C5675 0.22UF 20% 6.3V X5R 0201

PLACE NEAR U5000 C1 11MM

GND_SMC_AVSS

R5671 20K 5% 1/20W MF 201

Gain: 200x
Scale 0.25A / V
MAX VOUT 3V AT 0.825A
PLACEMENT NOTES
Place close to SMC
(For R and C)

VR IMON Current Sense Filter

CPUVR_IMON

R5641 0 5% 1/20W MF 0201

PLACE_NEAR U5000 B8 5MM

NO STUFF C5641 2NF 10% 16V X5R-CERM 0201

SMC_CPU_IMON_ISENSE

GND_SMC_AVSS

Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Discrete High side Current threshold

PP3V3_S0

BYPASS=U5601 3MM
C5613 0.1UF 10% 6.3V CERM X5R 0201

R5614 294K 1% 1/16W MF LF 402

R5615 49.9K 1% 1/16W MF LF 402

HS_COMP_VREF

R5616 10.2K 1% 1/16W MF LF 402

HS_COMP_FB

U5611 MCP6541T SC70-5

HS_COMP_OUT

NO STUFF C5611 0.22UF 20% 6.3V X5R 0201

R5619 255K 1% 1/16W MF LF 402

HS_IOUT_R

NOSTUFF C5610 0.1UF 10% 25V X5R 402

NOSTUFF R5617 0 5% 1/20W MF 0201

R5610 0 5% 1/20W MF 0201

HS_IOUT_D

NOSTUFF D5617 RB521ES-30

ISNS_HS_COMPUTING_IOUT

BMON : Discrete BMON Current Sense / Filter

PP3V3_S0

BYPASS=U5601 3MM
C5603 0.1UF 10% 6.3V CERM X5R 0201

R5604 100K 1% 1/16W MF LF 402

BMON_COMP_VREF

R5605 100K 1% 1/16W MF LF 402

R5606 10.2K 1% 1/16W MF LF 402

BMON_COMP_FB

U5601 MCP6541T SC70-5

NO STUFF C5601 0.22UF 20% 6.3V X5R 0201

R5609 200K 1% 1/16W MF 402

BMON_COMP_OUT

U5602 DMN32D2LFB4 DFN1006H4 3 SYM VER 2

SMC_BMON_COMP_ALERT_L

U5612 DMN32D2LFB4 DFN1006H4 3 SYM VER 2

SMC_HS_COMP_ALERT_L

Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

BMON_IOUT_R

NOSTUFF C5600 0.1UF 10% 25V X5R 402

NOSTUFF R5607 0 5% 1/20W MF 0201

R5600 0 5% 1/20W MF 0201

BMON_IOUT_D

NOSTUFF D5607 RB521ES-30

BYPASS=U5600:3MM
C5606 0.1UF 10% 6.3V CERM X5R 0201

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

U5600 INA213 SC70 CRITICAL (50V/V)

V+	6		
IN-	5	OUT	6
IN+	4	REF	1
GND	2		

CKPLUS WAIVE=NdifPr badTerm
CHGR_CSO_R_P
CHGR_CSO_R_N
CKPLUS WAIVE=NdifPr badTerm

BMON_IOUT

R5601 20K 5% 1/20W MF 201

PLACE_NEAR=U5000.A3:5MM

R5608 4.53K 1% 1/20W MF 201

SMC_BMON_DISCRETE_ISENSE

PLACE_NEAR=U5000.A3:5MM

C5602 0.22UF 20% 6.3V X5R 0201

GND_SMC_AVSS

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5675		PANEL ISNS NO

SYNC MASTER=J41_MLB SYNC DATE=03/28/2013

PAGE TITLE: Debug Sensors 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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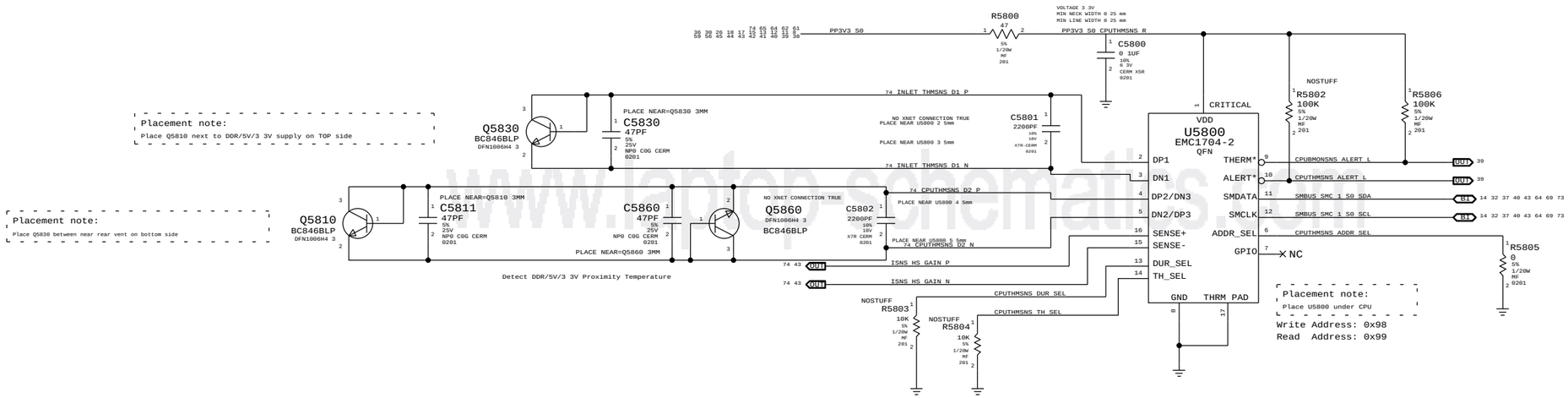
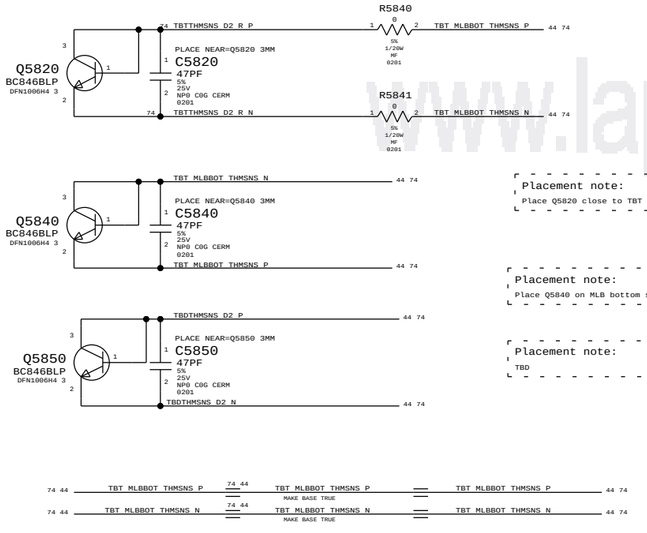
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors

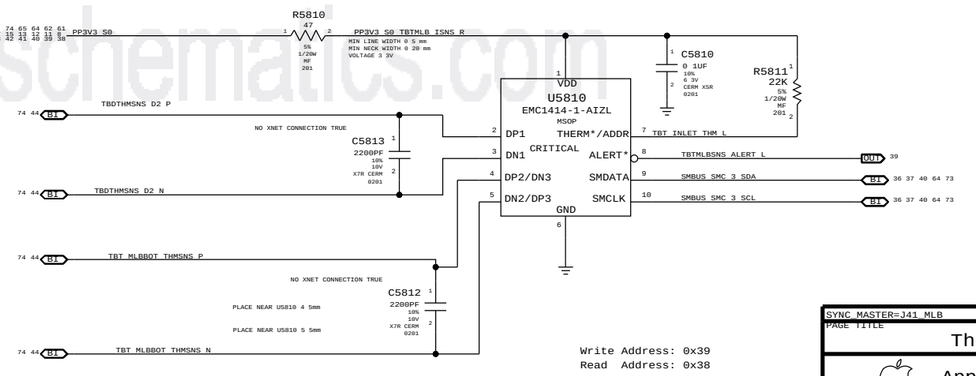


Placement note:
Place Q5820 close to TBT on TOP side

Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBD

TBT, MLBBOT and TBD Temp Sensor



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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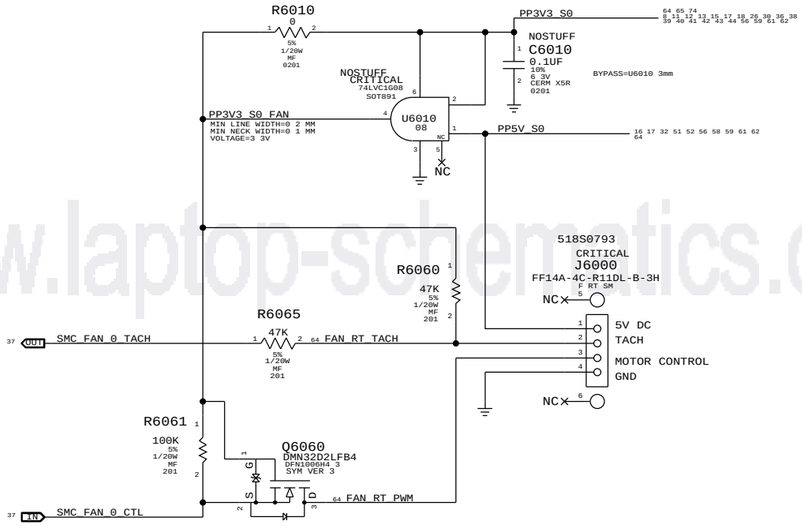
FAN CONNECTOR



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: Fan

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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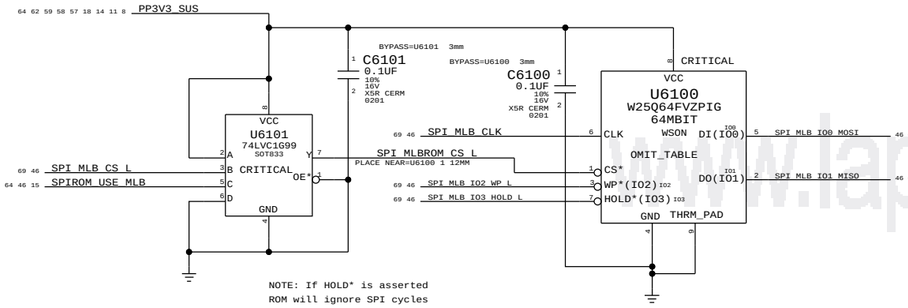
SPI ROM

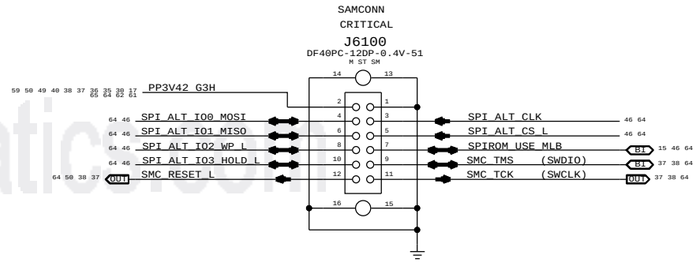
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

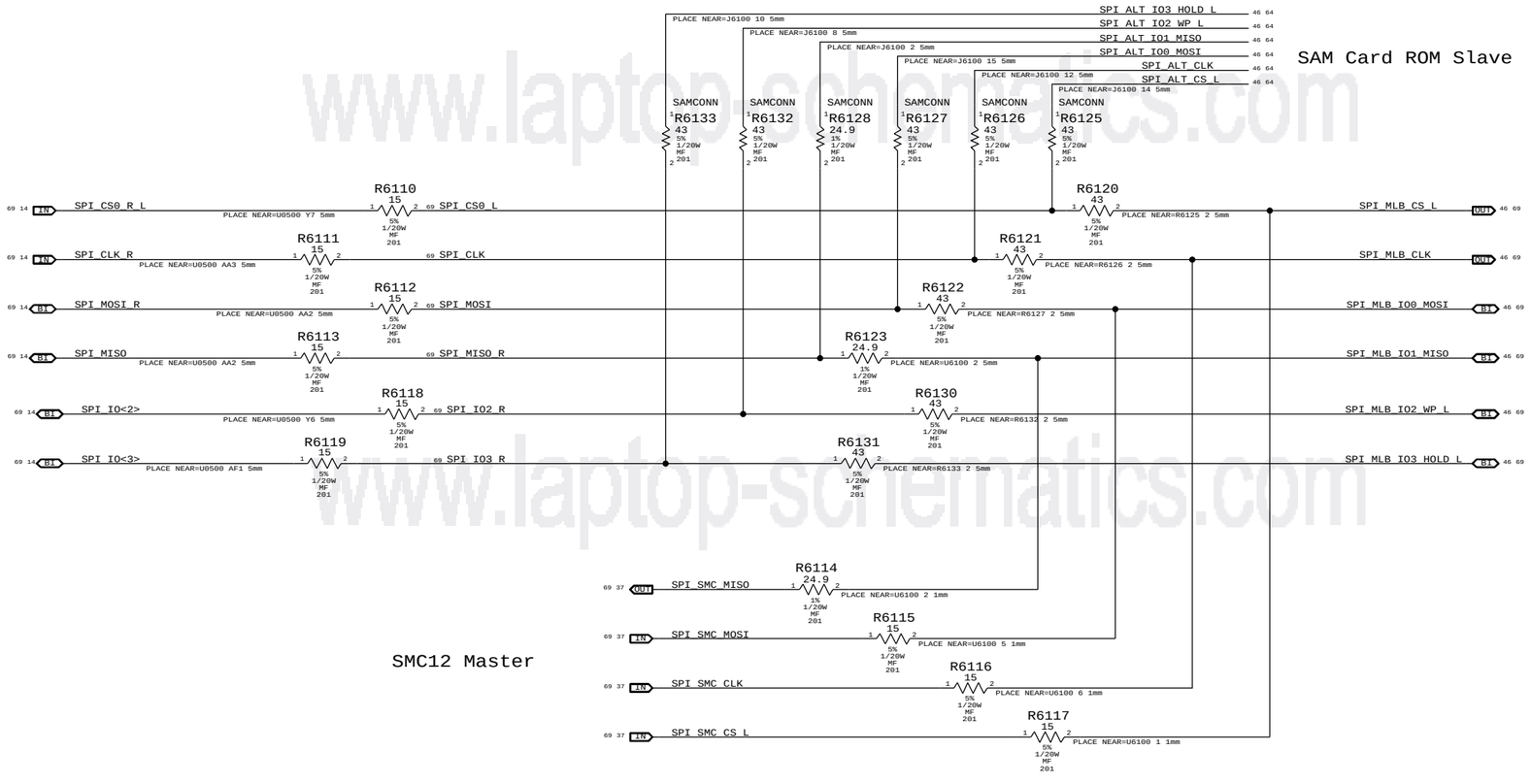
Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination

CPU Master



MLB ROM Slave

SMC12 Master

SAM Card ROM Slave

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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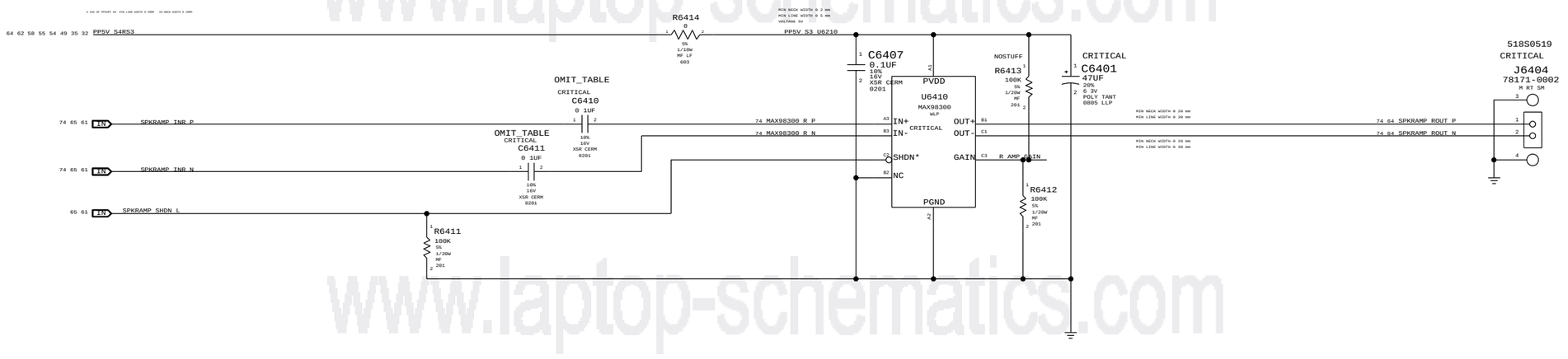
SPEAKER AMPLIFIERS

APN 353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0460	2	CAP CER XSR 0 1UF 10% 16V 0201 MURATA	C6410,C6411	CRITICAL	

SYNC_MASTER=J41_MLB SYNC_DATE=04/26/2013

PAGE TITLE: Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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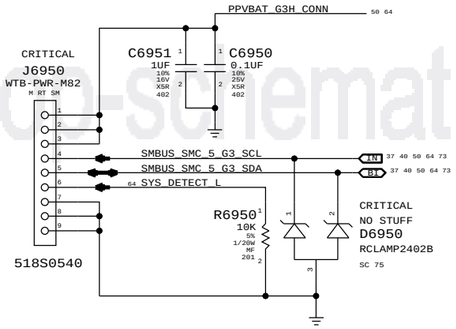
13" SPECIFIC

Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Battery Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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MLB to LIO Power Cable Connector

CRITICAL
J7000
WTB-PWR-M82
M RT SM

64 62 50 PPDCIN_G3H

PP5V_S4RS3 62 64 32 35 47 54 55 58

518S0508

C7006 0.1UF 10% 16V X5R CERM 0201

NO STUFF CRITICAL C7007 1UF 10% 35V X5R 603

NO STUFF CRITICAL C7008 1UF 10% 35V X5R 603

NO STUFF C7005 0.1UF 10% 50V X7R 603 1

R7012 68K 1% 1/20W MF 201

Input impedance of 68K meets sparkitecture requirements for detection of B121 (16.5V)

CRITICAL
Q7010
SI5419DU
POWERPAK

R7010 100K 5% 1/20W MF 201

CRITICAL C7012 0.047UF 10% 25V X7R 0402

R7011 10K 1% 1/20W MF 201

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

64 62 50 42 PPDCIN_G3H_ISOL

CRITICAL
D7012
SDZT15R6.8
0201
6.8V Zener

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

64 62 56 50 42 41 27 PPBUS_G3H

R7006 4.7 5% 1/8W MF LF 805
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=8.6V

PPBUS_G3H_R

CRITICAL
D7005
BAT30CWFILM
SOT 323

R7005 10 5% 1/8W MF LF 805
MIN LINE WIDTH=0.4 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=18.5V

PP18V5_DCIN_ISOL_R

PPVIN_G3H_P3V42G3H
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=18.5V

CRITICAL
U7090
LT3470AED
DFN

VIN BOOST SHDN* NC SW BIAS FB GND THRM PAD

P3V42G3H_BOOST
DIDT=TRUE
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm

C7094 0.22UF 10% 10V CERM 402

CRITICAL L7095 10UH 20% 0.85A 0.46OHM 2520

P3V42G3H_SHDN_L

P3V42G3H_SW
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
SWITCH NODE=TRUE
DIDT=TRUE

NCX

P3V42G3H_FB
MIN LINE WIDTH=0.2 mm
MIN NECK WIDTH=0.2 mm

PP3V42_G3H 17 30 35 36 37 38 40 46 50 60 61 62 64 65

Vout = 3.425V
300mA Max Output
(Switcher limit)

R7080 0 5% 1/20W MF 0201

NO STUFF R7081 49.9K 1% 1/20W MF 201

NO STUFF C7080 1000PF 5% 25V CERM 0402

CRITICAL C7091 1UF 10% 25V X5R 402

CRITICAL C7090 1UF 10% 25V X5R 402

CRITICAL C7092 5.6UF 20% 25V POLY TANT CASE B2 SM

C7095 22PF 5% 50V C0G 0201

<Ra> R7095 348K 1% 1/20W MF 201

<Rb> R7096 200K 1% 1/20W MF 201

CRITICAL C7099 10UF 20% 10V X5R CERM 0402 1

CRITICAL C7098 10UF 20% 10V X5R CERM 0402 1

Vout = 1.25V * (1 + Ra / Rb)

SYNC MASTER=J43 MLB SYNC DATE=09/13/2012

PAGE TITLE
DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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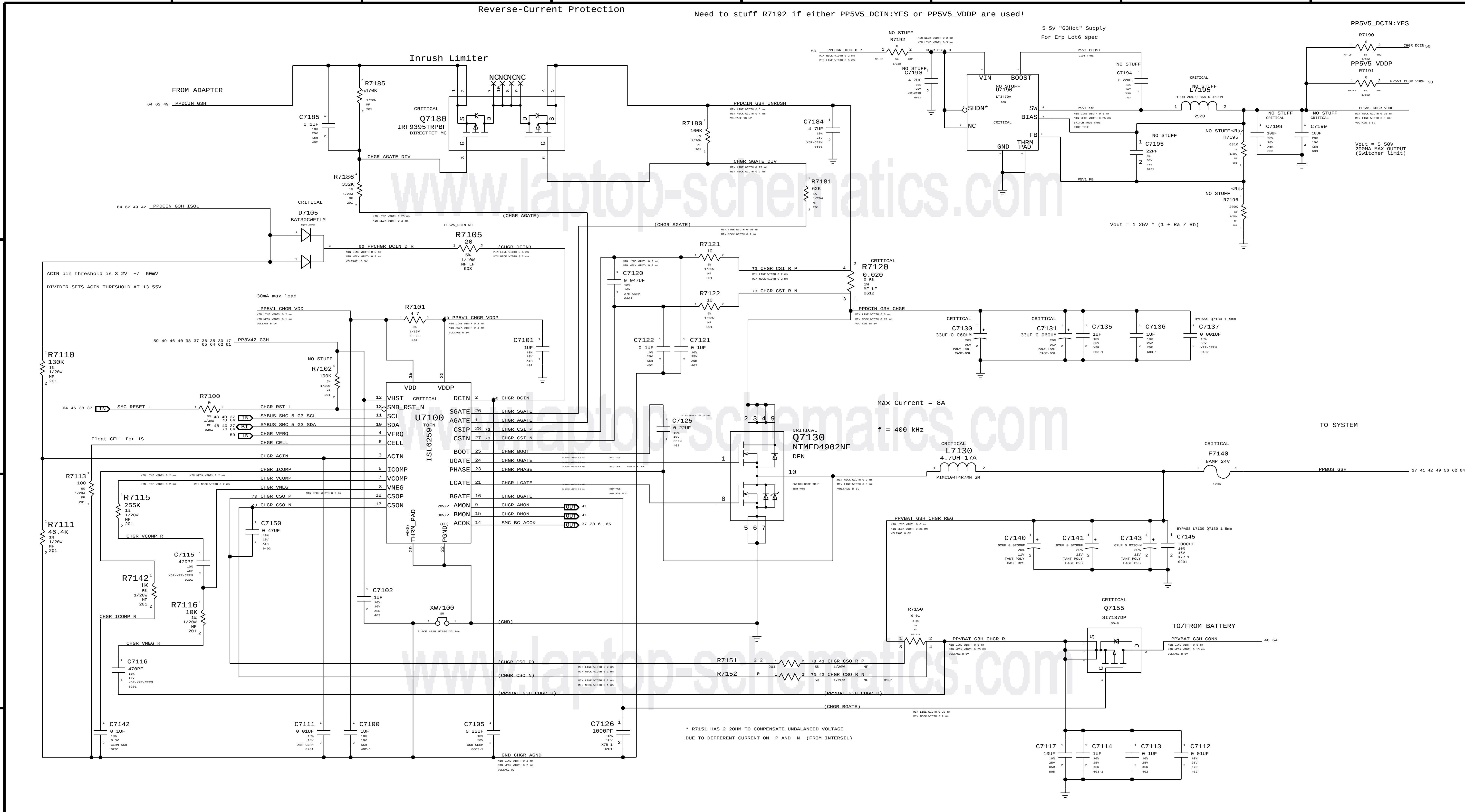


SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE

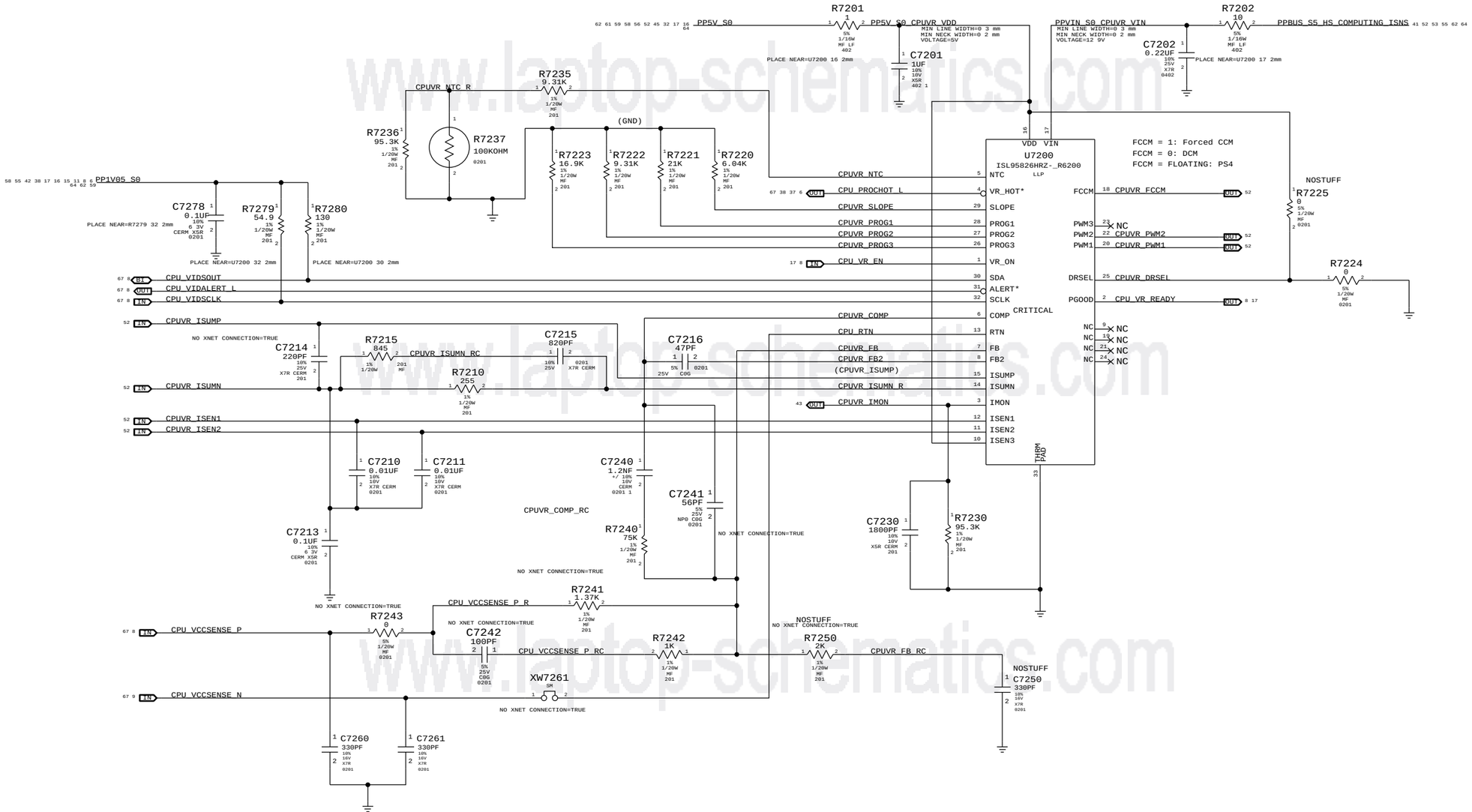
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>



SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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64 62 55 53 51 41 PPBUS_S5_HS_COMPUTING_ISNS

51 45 32 17 16 61 59 58 56 52 64 62 PP5V_S0

PHASE 1

C7310 1UF 10% 16V X6S CERM 0402

CPUVR_UGATE1 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

Q7310 SISA18DN PWRPAK SM — OMIT_TABLE, CRITICAL

U7310 ISL6208D DFN — CRITICAL

VCC, PWM, FCCM, BOOT, UGATE, PHASE, LGATE, THRM PAD, GND

51 IN CPUVR_PWM1

52 51 IN CPUVR_FCCM

353S3942

CPUVR_LGATE1 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

Q7311 SISA12DN PWRPAK SM — OMIT_TABLE, CRITICAL

CPUVR_BOOT1 — MIN LINE WIDTH=0.25 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

R7311 2.2 5% 1/16W MF LF 402

1CPUVR_BOOT1_RC — MIN LINE WIDTH=0.25 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

C7311 0.22UF 10% 16V CERM 402

CPUVR_PHASE1 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE, SWITCH NODE TRUE

L7310 0.40UH-20%-16A MPCG0730 SM 152S1757 — CRITICAL

PPVCC_S0_CPU_PH1 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.25 MM, VOLTAGE=1.8V

R7310 0 00075 1% 1W MF 0612 — CRITICAL

74 42 OUT CPUVR_ISNS1_P

CPUVR_ISNS1_N OUT 42 52 74

R7312 2.2 5% 1/10W MF LF 603 — NOSTUFF

R7314 1.00 1% 1/20W MF LF 0201

CPUVR_PH1_SNUB — DIDT TRUE, NOSTUFF

C7312 0.001UF 10% 50V X7R CERM 0402

CPUVR_ISUMN OUT 51 52 — NO XNET CONNECTION=TRUE

R7315 1K 1% 1/20W MF 201

R7316 200K 1% 1/20W MF 201

R7317 NOSTUFF — OMIT — NONE NONE NONE 0201

CPUVR_ISNS2_N 42 52 74 — NO XNET CONNECTION=TRUE

CPUVR_ISEN1 OUT 51

CPUVR_ISUMP OUT 51 52

C7313 CRITICAL; C7314 CRITICAL; C7315 NOSTUFF CRITICAL; C7316 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL; C7317 1UF 10% 16V X6S CERM 0402; C7318 0.001UF 10% 50V X7R CERM 0402; C7319 0.001UF 10% 50V X7R CERM 0402 — THESE TWO CAPS ARE FOR EMC

C7323 CRITICAL; C7324 CRITICAL; C7325 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL; C7326 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL; C7327 1UF 10% 16V X6S CERM 0402; C7328 0.001UF 10% 50V X7R CERM 0402; C7329 0.001UF 10% 50V X7R CERM 0402 — THESE TWO CAPS ARE FOR EMC

Additonal Input Bulk Caps

C7370 CRITICAL; C7371 CRITICAL; C7372 CRITICAL; C7373 CRITICAL; C7374 CRITICAL; C7375 CRITICAL; C7376 CRITICAL; C7377 CRITICAL — 620UF-0.023OHM 20% 11V TANT-POLY CASE-B2S

PPVCC_S0_CPU 8 10 42 62 64

Vout = 1.85V max
32A max output
f = 700kHz

61 59 58 56 52 51 45 32 17 16 64 62 PP5V_S0

PHASE 2

C7320 1UF 10% 16V X6S CERM 0402

CPUVR_UGATE2 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

Q7320 SISA18DN PWRPAK SM — OMIT_TABLE, CRITICAL

U7320 ISL6208D DFN — CRITICAL

VCC, PWM, FCCM, BOOT, UGATE, PHASE, LGATE, THRM PAD, GND

51 IN CPUVR_PWM2

52 51 IN CPUVR_FCCM

353S3942

CPUVR_LGATE2 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

Q7321 SISA12DN PWRPAK SM — OMIT_TABLE, CRITICAL

CPUVR_BOOT2 — MIN LINE WIDTH=0.25 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

R7321 2.2 5% 1/10W MF LF 402

CPUVR_BOOT2_RC — MIN LINE WIDTH=0.25 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE

C7321 0.22UF 10% 16V CERM 402

CPUVR_PHASE2 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.2 MM, DIDT TRUE, SWITCH NODE TRUE

L7320 0.40UH-20%-16A MPCG0730 SM 152S1757 — CRITICAL

PPVCC_S0_CPU_PH2 — MIN LINE WIDTH=0.6 MM, MIN NECK WIDTH=0.25 MM, VOLTAGE=1.8V

R7320 0 00075 1% 1W MF 0612 — CRITICAL

74 42 OUT CPUVR_ISNS2_P

CPUVR_ISNS2_N OUT 42 52 74

R7322 2.2 5% 1/10W MF LF 603 — NOSTUFF

R7324 1.00 1% 1/20W MF LF 0201

CPUVR_PH2_SNUB — DIDT TRUE, NOSTUFF

C7322 0.001UF 10% 50V X7R CERM 0402

CPUVR_ISUMN OUT 51 52 — NO XNET CONNECTION=TRUE

R7325 1K 1% 1/20W MF 201

R7326 200K 1% 1/20W MF 201

R7327 NOSTUFF — OMIT — NONE NONE NONE 0201

CPUVR_ISNS1_N 42 52 74 — NO XNET CONNECTION=TRUE

CPUVR_ISEN2 OUT 51

CPUVR_ISUMP OUT 51 52

SYNC_MASTER=J41_MLB SYNC_DATE=05/21/2013

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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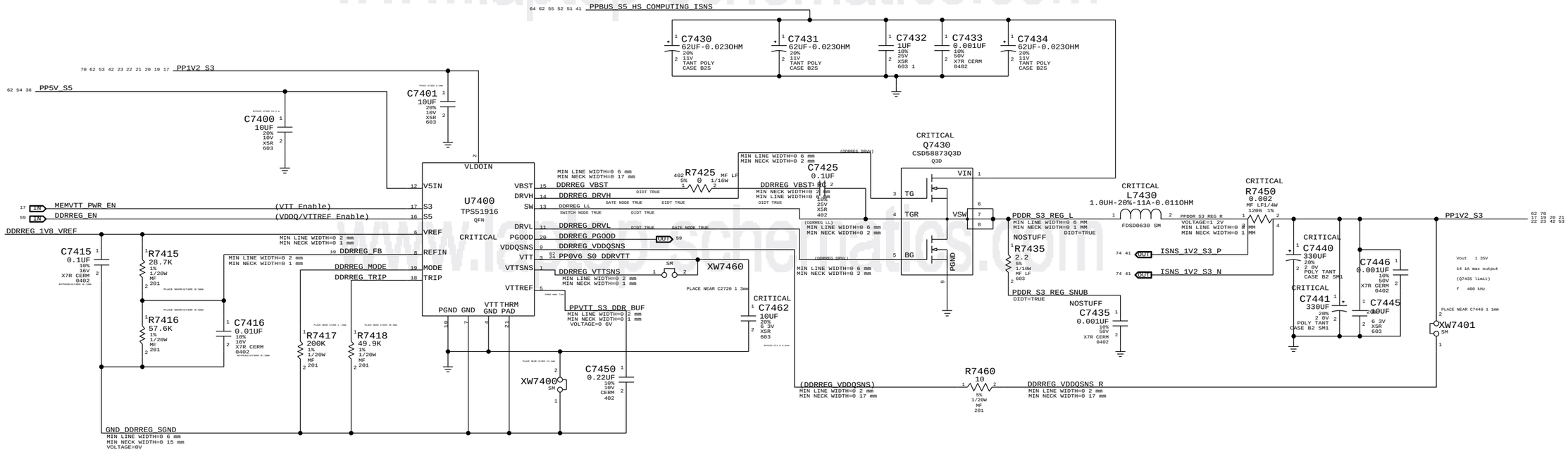

SYNC_MASTER=J41_MLB SYNC_DATE=05/21/2013

PAGE TITLE: LPDDR3 Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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SKIPSEL Strap		
VREF2	Auto Skip	(Higher Efficiency)
VREG3	OOA Auto Skip	(Lower Efficiency)

64 62 41 PPBUS S5 HS OTHER ISNS

BYPASS Q7520 1 1 5mm

C7542 62UF 0 023OHM

C7540 62UF 0 023OHM

C7570 100PF 10% 16V X7R 1 0201

C7541 1UF 10% 16V X5R 402

C7500 1UF 10% 16V X5R 402

62 53 32 PPDV S5

62 58 55 54 49 47 35 32 64 PPSV S4RS3

54 PSVP3V3 VREG3

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 2 mm

54 PSVP3V3 VREF2

R7500 0 1% 1/20W MF 0201

NOSTUFF R7501 0 1% 1/20W MF 0201

C7501 0 22UF 10% 16V CERM 402

C7503 2 2UF 20% 16V CERM 402

C7505 10UF 20% 6 3V X5R 603

C7584 62UF 0 023OHM

C7582 62UF 0 023OHM

C7581 1UF 10% 16V X5R 402

C7583 1000PF 10% 16V X7R 1 0201

BYPASS Q7560 1 1 5mm

F=400KHZ

58 55 54 49 47 35 32 64 62 PPSV S4RS3

Vout = 5 0V

7 2A MAX OUTPUT

Q7520 CSD58873Q3D Q3D

VIN TG TGR BG VSW PGND

CRITICAL L7520 2.2UH-20%-9A-0.012OHM PIME063T2R2MS SM 152S1798

PSV S4RS3 REG L DIDT TRUE

PLACE NEAR L7520 1 3mm

PLACE NEAR L7520 2 3mm

XW7520 XW7521

C7554 62UF 20% 6 3V ELEC CASE-B2S

C7552 150UF 0 035OHM 20% 6 3V POLY-TANT CASE-B2-SM

C7550 10UF 20% 6 3V X5R 603

C7551 1000PF 10% 16V X7R 1 0201

PLACE NEAR L7520 1 1 5mm

PLACE NEAR L7520 1 3mm

NOSTUFF R7522 2.2 5% 1/10W MF LF 603

PSV S4RS3 REG SNUB DIDT=TRUE

NOSTUFF C7522 0.001UF 10% 50V X7R CERM 0402

PSV S4RS3 VFB1 XW MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

R7523 10 5% 1/20W MF 201

PSV S4RS3 VFB1 R

R7520 41 2K 1% 1/20W MF 201

R7521 10K 1% 1/20W MF 201

PSV S4RS3 VBST R MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

C7524 0 1UF 10% 25V X5R 402

R7545 0 5% 1/16W MF-LF 402

PSV S4RS3 CSP1 R DIDT TRUE MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

C7518 0 1UF 10% 16V X7R-CERM 0402

R7547 1 33K 1% 1/20W MF 201

R7556 4 22K 1% 1/20W MF 201

PSV S4RS3 COMP1 R

R7536 7 5K 1% 1/20W MF 201

NO STUFF R7537 20K 1% 1/20W MF 201

C7536 4700PF 10% 16V X7R 201

C7537 270PF 10% 16V X7R-CERM 0201-1

R7549 0 1% 1/20W MF 0201

54 PSVP3V3 VREF2

59 OUT PSVS4RS3 PGOOD

59 37 OUT S5_PWRGD

GND PSVP3V3_SGND MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm VOL_AGE 0V

PLACE_NEAR U7501 4 2mm

R7551 0 5% 1/20W MF 0201

59 EN PSVS4RS3 EN

CRITICAL U7501 TPS51980A QFN

VSW VIN VREG5 VREG3 VREF2

SKIPSEL1 SKIPSEL2 OCSEL VBST1 DRVH1 SW1 DRVL1 CSP1 CSN1 MODE VFB1 COMP1 EN1 PGOOD1 GND THRM_PAD

EN VBST2 DRVH2 SW2 DRVL2 CSP2 CSN2 RF VFB2 COMP2 EN2 PGOOD2

12 SMC_PM_G2_EN 37 38 59

P3V3_S5_VBST P3V3_S5_DRVH P3V3_S5_LL P3V3_S5_DRVL P3V3_S5_CSP2 P3V3_S5_CSN2 P3V3_S5_RF P3V3_S5_VFB2 P3V3_S5_COMP2 P3V3S5_EN_R

PLACE_NEAR U7501 25 2mm

R7552 0 5% 1/20W MF 0201

59 EN S5_PWR_EN

Q7560 CSD58873Q3D Q3D

VIN TG TGR BG VSW PGND

P3V3_S5_VBST_R MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

R7564 0 5% 1/16W MF-LF 402

C7564 0 1UF 10% 25V X5R 402

MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

C7588 0 1UF 10% 16V X7R-CERM 0402

R7546 1 54K 1% 1/20W MF 201

R7516 6 65K 1% 1/20W MF 201

R7506 240K 1% 1/20W MF 201

R7538 7 5K 1% 1/20W MF 201

R7539 20K 1% 1/20W MF 201

C7538 4700PF 10% 16V X7R 201

C7539 22PF 5% 6 3V NPO-COG 0201

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

P3V3_S5_CSP2_R DIDT TRUE

P3V3_S5_COMP2_R

54 PSVP3V3 VREF2

P3V3_S5_VBST_R MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 2 mm DIDT TRUE

P3V3_S5_REG_L DIDT TRUE

CRITICAL L7560 2 2UH 20% 9A 9 012OHM PIME063T2R2MS-SM 152S1798

PLACE NEAR L7560 1 3mm

PLACE NEAR L7560 2 3mm

XW7560 XW7561 XW7562

NOSTUFF R7562 2.2 5% 1/10W MF LF 603

P3V3_S5_REG_SNUB DIDT=TRUE

NOSTUFF C7562 0.001UF 10% 50V X7R CERM 0402

C7590 100UF 20% 6 3V X5R 603

C7592 150UF 0 018OHM 1 8A POLY-TANT CASE-B2-SM

C7593 150UF 0 018OHM 1 8A POLY-TANT CASE-B2-SM

C7572 1000PF 10% 16V X7R 1 0201

C7594 150UF 0 018OHM 1 8A POLY-TANT CASE-B2-SM

PLACE NEAR L7560 2 1 mm

PP3V3_S5_REG_R Vout = 3 3V 6 5A MAX OUTPUT F=400KHZ

P3V3_S5_VFB2_XW MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

R7563 10 5% 1/20W MF 201

P3V3_S5_VFB2_R MIN LINE WIDTH 0 2 mm MIN NECK WIDTH 0 1 mm

R7560 23 2K 1% 1/20W MF 201

R7561 10K 1% 1/20W MF 201

SYNC_MASTER=J41_MLB SYNC_DATE=09/17/2012

PAGE TITLE: 5V S4RS3 / 3.3V S5 Power Supply

Apple Inc.

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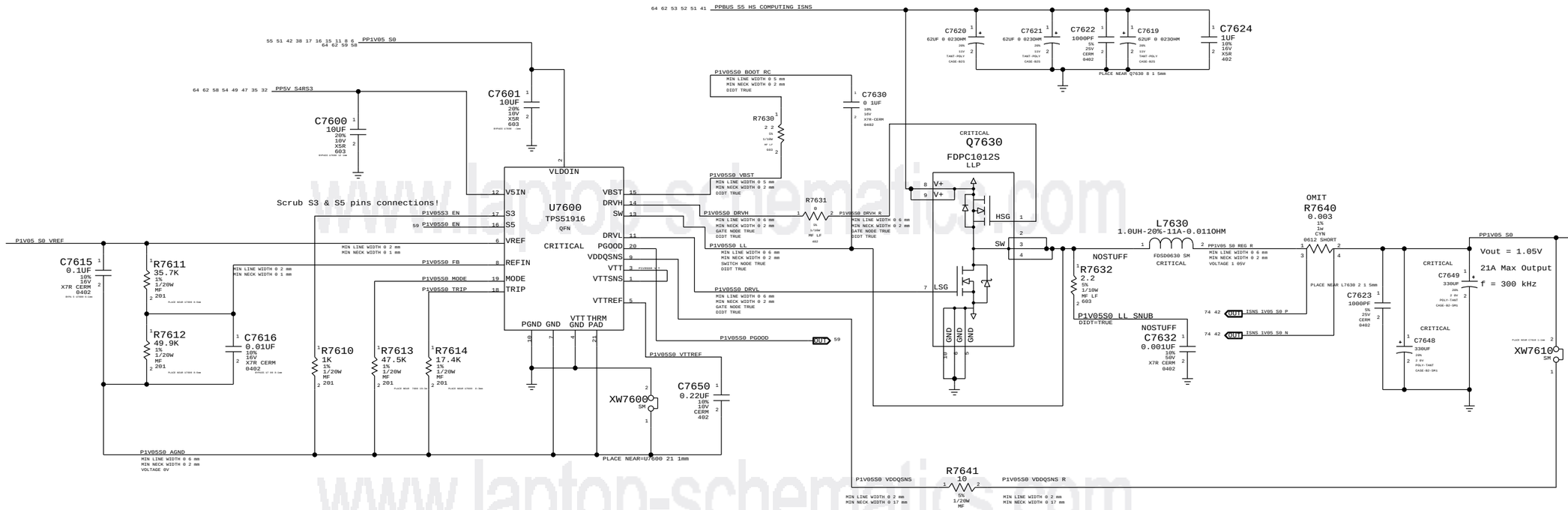
1.05V S0 Regulator



SYNC_MASTER=J41_MLB SYNC_DATE=05/21/2013

PAGE TITLE: 1.05V S0 Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P TYPE
RDS(ON)	43 mOhm @4 5V
LOADING	0 65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T BONE FOR ACOUSTICS
*PPBUS SW LCDBKLT PWR SW SHOULD BE KEPT AS SHORT AS POSSIBLE
*LCD BKLT PWM SHOULD BE AWAY FROM BOOST CIRCUIT

CRITICAL Q7706 FDC638APZ_SBMS001 SSOT6 HF

F7700 3AMP-32V-467 603 HF PLACE SIDE=BOTTOM

PPBUS_G3H — PPVIN_S0SW_LCDBKLTFET — PPVIN_S0SW_LCDBKLT_FET

THERE IS A SENSE RESISTOR BETWEEN PPBUS SW LCDBKLT PWR AND PPBUS SW BKL ON THE SENSOR PAGE

R7788 301K 1% 1/20W MF 201
C7782 0.1UF 10% 16V X7R CERM 0402
LCDBKLT_EN_DIV_L
R7789 147K 1% 1/20W MF 201
LCDBKLT_EN_L

Q7707 DMN5L06VK-7 SOT563 VER 3
EDP_BKLT_EN — LCDBKLT_DISABLE
Q7707 DMN5L06VK-7 SOT563 VER 3
BKLT_PLT_RST_L

CRITICAL L7701 15UH-2.8A PIMB053T SM
PPVIN_S0SW_LCDBKLT — LCDBKLT_BOOST
MIN LINE WIDTH=0 5 MM
MIN NECK WIDTH=0 150 MM
VOLTAGE=50V
SWITCH NODE=TRUE
DIDT=TRUE

CRITICAL C7712 10UF 10% 25V X5R 805
CRITICAL C7713 0.1UF 10% 25V X5R 402
PLACE NEAR=L7701 1 3mm

CRITICAL D7701 SOD 123 RB160M-60G
PLACE NEAR=L7701 2 3mm
C7796 220PF 10% 50V X7R CERM 0402
CRITICAL C7797 10UF 10% 50V X5R 1210 1
CRITICAL C7799 10UF 10% 50V X5R 1210 1
PPHV_S0SW_LCDBKLT
PLACE NEAR=U7701 A5 3mm
PLACE NEAR=D7701 2 3mm
PLACE NEAR=D7701 2 5mm

PP5V_S0
C7710 1UF 10% 25V X5R 603 1
BYPASS=U7701 D1 5mm
C7714 0.01UF 10% 10V X5R CERM 0201
BYPASS=U7701 D1 3mm

XW7720 SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN LINE WIDTH=0 1 MM
MIN NECK WIDTH=0 1 MM
PLACE NEAR=C7797 1 5mm

PP3V3_S0
BYPASS=U7701 C4 4mm
C7711 0.1UF 10% 6 3V CERM X5R 0201

(GND_BKL_SGND)

U7701 25 BUMP MICRO LP8559
VDDIO VLDO VIN

BKL_VSYNC_R	D2	VSYNC	
BKL_FLTR	C2	FILTER	
BKL_ISET	B3	ISET	
BKL_FSET	B4	FSET	
BKL_SCL	D3	SCLK	
BKL_SDA	D4	SDA	
BKL_PWM	A4	PWM	
BKL_EN	A3	EN	
BKL_FAULT	C3	FAULT	
		SW_0	B1
		SW_1	B2
		FB	A5
		OUT1	E5 BKL_ISEN1
		OUT2	D5 BKL_ISEN2
		OUT3	C5 BKL_ISEN3
		OUT4	E3 BKL_ISEN4
		OUT5	E2 BKL_ISEN5
		OUT6	E1 BKL_ISEN6
		GND_S	B5
		GND_L	E4
		GND_SW	A1
		GND_SW	A2

SMBUS_PCH_CLK — R7753 0 5% 1/20W MF 0201
SMBUS_PCH_DATA — R7757 0 5% 1/20W MF 0201
Addr: 0x58(Wr)/0x59(Rd)

R7741 10K 5% 1/20W MF 201

PPVIN_S0SW_LCDBKLT
R7731 200K 1% 1/20W MF 201
R7715 100K 1% 1/20W MF 201

EDP_BKLT_PWM — R7704 33 5% 1/20W MF 201
C7704 33PF 5% 25V NP0 C0G 0201

TP7701 TP P6 PLACE SIDE=BOTTOM

I_LED=17.1mA
Fpwm=9.62kHz see spec for others

R7755 10K 5% 1/20W MF 201
R7714 21.5K 1% 1/20W MF 201
R7716 90.9K 1% 1/20W MF 201

XW7710 SM
GND_BKL_SGND MIN LINE WIDTH=0 4 MM MIN NECK WIDTH=0 2 MM VOLTAGE=0V

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES THIN FLIM 1/16W 10 2 OHM 0 1 0402 SM	R7717 R718 R7719		BKLT:ENG
103S0198	3	RES THIN FLIM 1/16W 10 2 OHM 0 1 0402 SM	R7720 R7721 R7722		BKLT:ENG

R7717 0 — BKLT:PROD — LED_RETURN_1 — OUT 60 64
R7718 0 — BKLT:PROD — LED_RETURN_2 — OUT 60 64
R7719 0 — BKLT:PROD — LED_RETURN_3 — OUT 60 64
R7720 0 — BKLT:PROD — LED_RETURN_4 — OUT 60 64
R7721 0 — BKLT:PROD — LED_RETURN_5 — OUT 60 64
R7722 0 — BKLT:PROD — LED_RETURN_6 — OUT 60 64
5% 1/16W MF LF 402
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 20 mm
PLACE NEAR=U7701 E5 10mm / D5 10mm / C5 10mm / E3 10mm / E2 10mm / E1 10mm

PLACEMENT NOTE=Keep away from noise nodes(E4 A1 A2 B1 B2 pins)

Keyboard Backlight Driver & Detection

PP5V_S0 — BYPASS=U7750 1 2 2 MM
CRITICAL L7750 10UH-0.58A-0.35OHM 1098AS SM
KBDLED_SW MIN LINE WIDTH=0 3 MM MIN NECK WIDTH=0 225 MM SWITCH NODE=TRUE DIDT=TRUE
C7750 1UF 10% 10V XSR 402

U7750 SPN035007G MLF CRITICAL
VIN — EN — SW — FB — NC — OUT — GND — THRM PAD

SMC_SYS_KBDLED
KBDLED_FB MIN LINE WIDTH=0 25 MM MIN NECK WIDTH=0 2 MM VOLTAGE=40V
KBDLED_ANODE MIN LINE WIDTH=0 25 MM MIN NECK WIDTH=0 2 MM VOLTAGE=40V
R7700 4.7 5% 1/16W MF LF 402
C7755 0.22UF 10% 50V XSR CERM 0603 1
C7756 0.22UF 10% 50V XSR CERM 0603 1

Keyboard Backlight Connector

CRITICAL J7715 FF14A-4C-R11DL-B-3H F RT SM
NC — NC
518S0793

SYNC_MASTER=J43_MLB	SYNC_DATE=09/13/2012
PAGE TITLE	LCD/KBD Backlight Driver
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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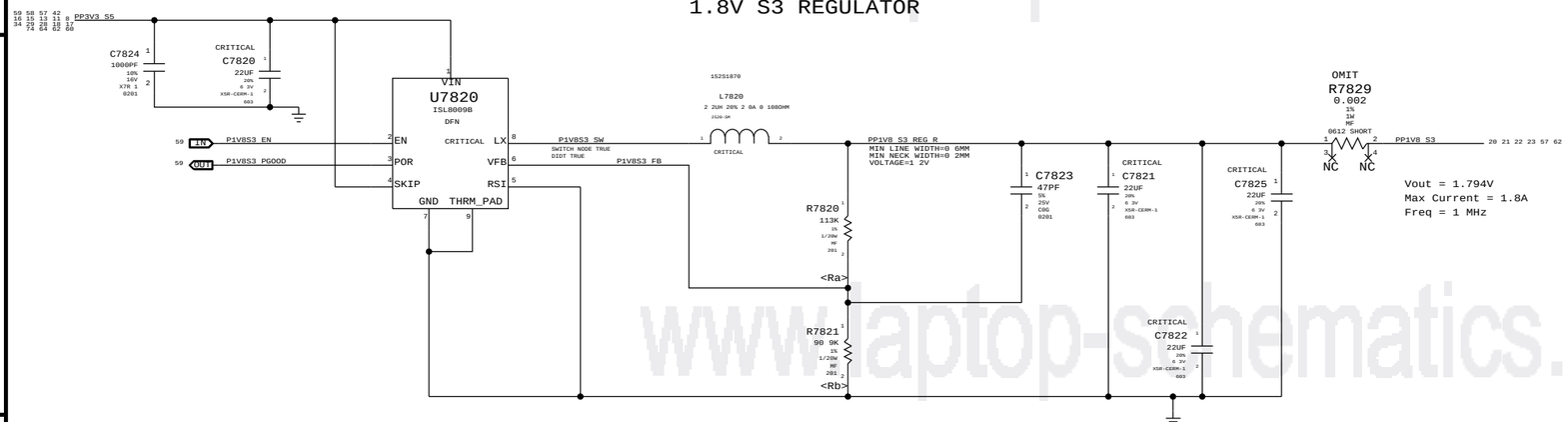
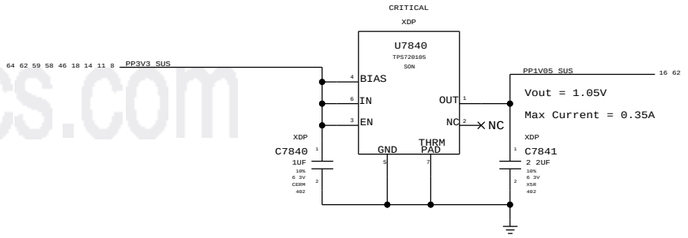
1.8V S3 REGULATOR

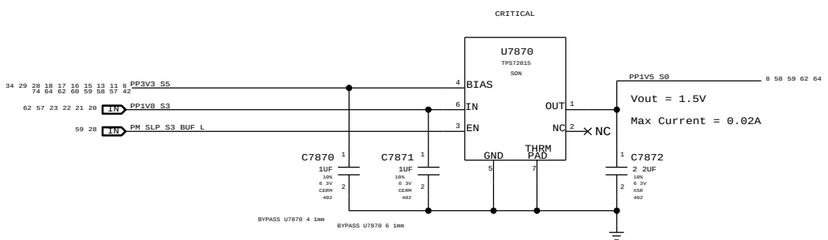


1.05V SUS LDO

Cougar Point requires JTAG pull ups to be powered at 1 05V when SUS suspend well is active
Pull ups (3) must be 51 ohms to support XDP (not required in production)
70mA is required to support pull ups Alternative is strong voltage
dividers (200/100) to 3 3V S5 which burns 100mW in all S states



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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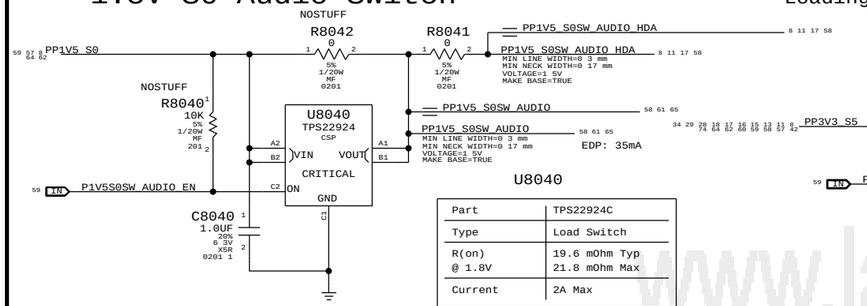
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

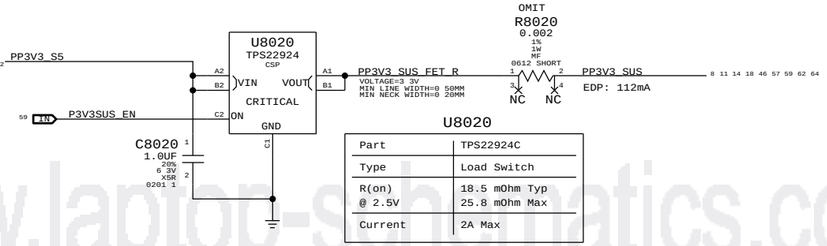
1.5V S0 Audio Switch



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

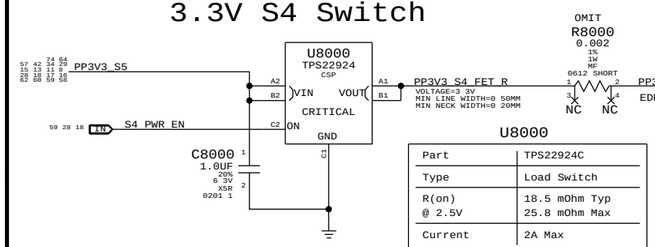
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

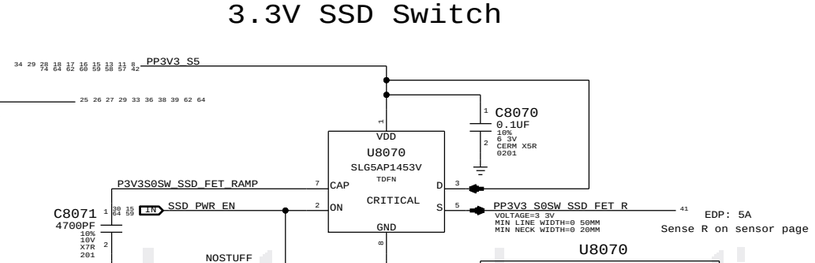
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

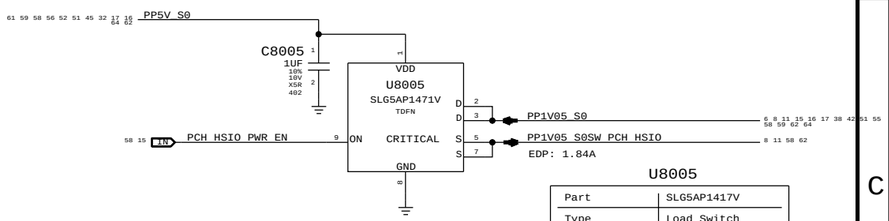
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

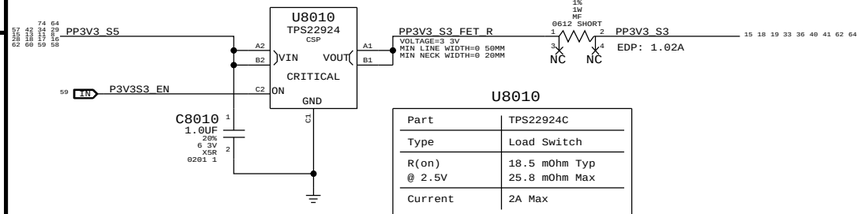


U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

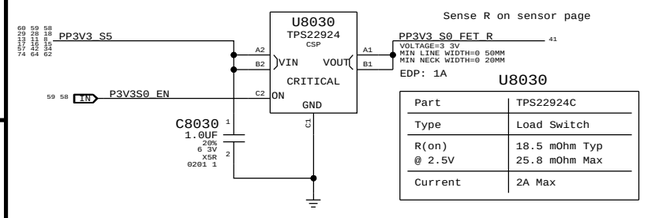
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

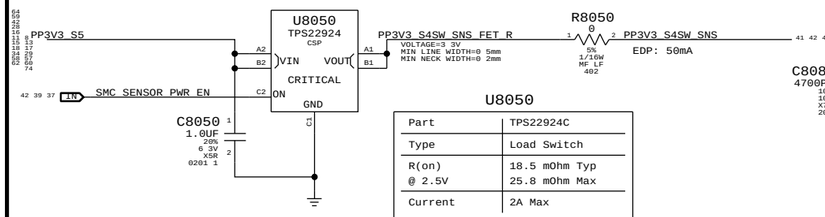
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

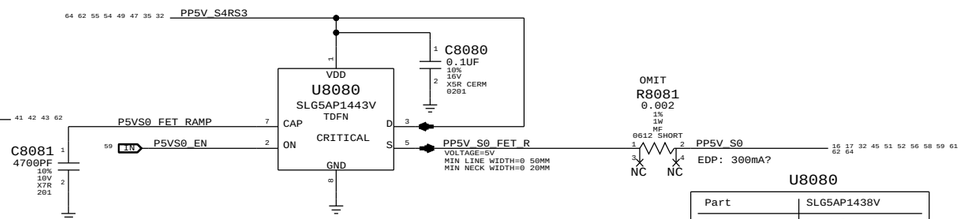
3.3V Sensor Switch



U8050

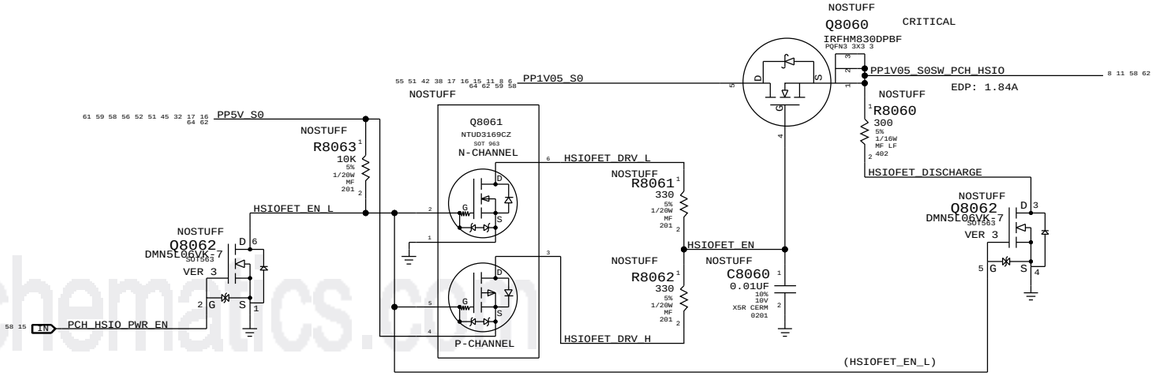
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	Power FETs
	Apple Inc.
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S5 Enables

SMC_PM_G2_EN (OUT) → R8140 100 5% 1/20W MF 201 → SMC_PM_G2_EN (IN), MAKE BASE=TRUE
S5_PWR_EN, MAKE BASE=TRUE → S5_PWR_EN (OUT)
NOSTUFF C8142 0.47UF 10% 6.3V CERM X5R 402, PLACE NEAR=U7501 21 7mm

S5 Power Good

PP3V42_G3H, PLACE NEAR=U7501 20 7mm
R8141 100K 5% 1/20W MF 201
S5_PWRGD >SMC
SMC >PM_DSW_PWRGD
S5_PWRGD, MAKE BASE=TRUE

SSD Enable

SSD_PWR_EN (IN), MAKE BASE=TRUE → SSD_PWR_EN (OUT)

Standby Enables

PP3V3_S5
NOSTUFF C8170 0.1UF 10% 6.3V CERM X5R 0201, BYPASS=U8170 6 2 3mm
NOSTUFF U8170 74LVC1G32 SOT891
PM_SLP_S5_L (IN)
SMC_S4_WAKESRC_EN (IN)
S4_PWR_EN, MAKE BASE=TRUE → S4_PWR_EN (OUT) ×2
R8115 0 5% 1/20W MF 0201

USB_PWR:STBY
R8114 100 5% 1/20W MF 201
USB_PWR:S3
R8117 100 5% 1/20W MF 201
USB_PWR_EN, MAKE BASE=TRUE → USB_PWR_EN (OUT)
NO STUFF C8114 0.47UF 10% 6.3V CERM X5R 402

USB_PWR:STBY
R8177 0 5% 1/20W MF 0201
S4_PWR_EN
USB_PWR:S3
R8179 0 5% 1/20W MF 0201
PM_SLP_S4_L
P5VS4RS3_EN_RC
NO STUFF D8175 0201 RB521ES-30
R8175 0 5% 1/20W MF 0201
NO STUFF R8176 240 5% 1/20W MF 201
P5VS4RS3_EN_D
P5VS4RS3_EN (OUT)
5V needs to be held up so 1.05V can fall after 1.5V
NO STUFF C8175 2.2UF 10% 6.3V X5R 402

PP3V3_S5
C8180 0.1UF 10% 6.3V CERM X5R 0201, BYPASS U8180 6 3mm
PM_SLP_S3_L (IN) → R8178 100 5% 1/20W MF 201 → PM_SLP_S3_R_L
U8180 MC74VHC1G08 SC70 HF
PM_SLP_S3_BUF_L, MAKE BASE=TRUE
NOSTUFF R8180 330K 5% 1/20W MF 201

S3 Enables

PM_SLP_S4_L (IN)
R8111 20K 5% 1/20W MF 201
R8116 0 5% 1/20W MF 0201
R8112 0 5% 1/20W MF 0201
C8111 0.1UF 20% 10V CERM 402
NO STUFF C8116 0.47UF 10% 6.3V CERM X5R 402
NO STUFF C8112 0.47UF 10% 6.3V CERM X5R 402
P3V3S3_EN, MAKE BASE=TRUE → P3V3S3_EN (OUT)
P1V8S3_EN, MAKE BASE=TRUE → P1V8S3_EN (OUT)
DDRREG_EN, MAKE BASE=TRUE → DDRREG_EN (OUT)

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (S3mAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (S3mA)	1	0	0	0	0	0	0

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K 1% 1/20W MF 201 → VMON_5V_DIV (5.0V Divider 1.07V) → R8152 15K 1% 1/20W MF 201
PP3V3_S5 → R8156 150K 1% 1/20W MF 201 → S0PGD_C
R8153 1K 5% 1/20W MF 201 → C8159 1UF 10% 10V X5R 402 (9ms RC delay)
PP3V3_S0 → R8158 15K 1% 1/20W MF 201 → VMON_3V3_DIV (3.3V Divider 1.07V) → R8159 7.15K 1% 1/20W MF 201
R8154 1K 5% 1/20W MF 201 → VMON_Q3_BASE
PP1V5_S0 → R8155 1K 5% 1/20W MF 201 → VMON_Q4_BASE
VMON_Q2_BASE, NC, NC
CRITICAL Q8150 ASMCC0179 DFN2015H4 8 376S0854 (Q1, Q2, Q3, Q4)
S0PGD_BJT_GND_R → R8157 100 5% 1/20W MF 201 → ALL_SYS_PWRGD (OUT)
Vbe 0.7V max @ 2mA
Vce(sat) 0.1V max @ 1mA
Q1 Vth 0.7~1V @Id 250uA

1.5V Codec Enable

PLACE NEAR=U8040 2 C7mm
AUD_PWR_EN (IN) → R8145 100K 5% 1/20W MF 201 → P1V5S0SW → AUDIO_EN (OUT)
D8146 0201 RB521ES-30, P1V5CODEC_EN_D, PLACE NEAR=U8040 2 C7mm
R8146 1K 5% 1/20W MF 201
C8146 0.1UF 10% 25V X5R 402, PLACE NEAR=U8040 C2 7mm

3.3V SUS Detect

PP3V3_S5, BYPASS U8130 6 2 3mm
No stuff C8131 12ms Min delay time
U8130 Sense input threhold is 3.07V
C8130 0.1UF 10% 6.3V CERM X5R 0201
PP3V3_SUS → R8133 100K 5% 1/20W MF 201 (OUT)
CRITICAL
U8130 TPS3808G33 QFN
PP3V3_SUS → SENSE
RESET* → PM_RSMRST_L (OUT)
MR* → TP_SUS_PGOOD_MR_L
SUS_PGOOD_CT → CT
GND, THRM PAD
NO STUFF C8131 1000PF 10% 16V X7R 1 0201

CHGR VFRQ Generation

PP3V42_G3H
R8131 330K 5% 1/20W MF 201
VFRQ Low Fix Frequency
VFRQ High Variable Frequency
CHGR_VFRQ (OUT)
Q8131 DMN32D2LFB4 DFN1006H4 3 SYM VER 2
PM_SLP_S3_R_L

S0 Enables

PM_SLP_S3_BUF_L, MAKE BASE=TRUE → PM_SLP_S3_BUF_L (OUT) ×2
NO STUFF D8185 0201 RB521ES-30
R8185 0 5% 1/20W MF 0201
R8184 330 5% 1/20W MF 201
D8184 0201 RB521ES-30
R8186 20K 5% 1/20W MF 201
R8187 0 5% 1/20W MF 0201
P1V05_EN_D → NO STUFF R8138 820 5% 1/20W MF 201
P3V3S0_EN_D
P5VS0_EN, MAKE BASE=TRUE → P5VS0_EN (OUT)
P3V3S0_EN, MAKE BASE=TRUE → P3V3S0_EN (OUT)
P1V05S0_EN, MAKE BASE=TRUE → P1V05S0_EN (OUT)
NO STUFF C8185 0.22UF 10% 6.3V CERM 402
C8186 0.1UF 20% 10V CERM 402
NO STUFF C8187 0.68UF 10% 6.3V CERM 402

SUS Enables

PM_SLP_SUS_L (IN), MAKE BASE=TRUE → PM_SLP_SUS_L (OUT)
R8190 0 5% 1/20W MF 0201
P3V3SUS_EN, MAKE BASE=TRUE → P3V3SUS_EN (OUT)
NO STUFF C8190 0.1UF 10% 25V X5R 402

S0 Rail PGOOD Circuitry (ISL version used for development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP1V05_S0 → R8160 6.04K 1% 1/20W MF 201 → 5V Divider 3 19V @ 4 5Vmin
PP5V_S0 → R8170 15K 1% 1/20W MF 201 → 1 5V Divider 0 718V @ 1 45Vmin
PP3V3_S0 → R8172 6.04K 1% 1/20W MF 201 → 1 05V Divider 0 723V @ 1 02Vmin
R8161 15K 1% 1/20W MF 201
R8171 15K 1% 1/20W MF 201
R8173 15K 1% 1/20W MF 201
S0PGOOD ISL
U8160 ISL88042IRTEZ TDFN
VDD, V2MON, V3MON, V4MON, GND, THRM PAD
P5V_DIV_VMON, P1V5_DIV_VMON, P1V05_DIV_VMON
MR* (IPU) → 353S2310 → NC
RST* → ALL_SYS_PWRGD_R
C8160 0.1UF 10% 6.3V CERM X5R 0201
R8162 330 5% 1/20W MF 201 → ALL_SYS_PWRGD (OUT)

P1V8S3_PGOOD (IN) → R8166 100 5% 1/20W MF 201
P5VS4RS3_PGOOD (IN) → R8165 100 5% 1/20W MF 201
P1V05S0_PGOOD (IN) → R8164 100 5% 1/20W MF 201
DDRREG_PGOOD (IN) → R8168 100 5% 1/20W MF 201
S0PGOOD_ISL → R8162 330 5% 1/20W MF 201 → ALL_SYS_PWRGD (OUT)
PM_SLP_S3_BUF_L → R8167 10K 5% 1/20W MF 201

SYNC_MASTER=J43_MLB	SYNC_DATE=09/16/2013
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LCD Connector

Internal DP Connector: 518S0829

CRITICAL

J8300

20525-130E-01

F RT SM

Pull-ups on panel side, 4.7 kOhm to 3.3V

R8363 4.7K 5% 1/20W MF 201

R8364 4.7K 5% 1/20W MF 201

R8361 0 5% 1/20W MF 0201

R8362 0 5% 1/20W MF 0201

73 40 37 BI SMBUS_SMC_0_S0_SDA — 64 I2C_TCON_SDA_R

73 40 37 BI SMBUS_SMC_0_S0_SCL — 64 I2C_TCON_SCL_R

64 62 56 PPHV_S0SW_LCDBKLT

64 56 OUT LED_RETURN_6

64 56 OUT LED_RETURN_5

64 56 OUT LED_RETURN_4

64 56 OUT LED_RETURN_3

64 56 OUT LED_RETURN_2

64 56 OUT LED_RETURN_1

LED Backlight I/F

DisplayPort I/F

NC NC NC NC NC

13 OUT DP_INT_HPD — R8360 0 5% 1/20W MF 0201 — 64 DP_INT_HPD_CONN

34 29 28 18 17 16 15 13 11 8 74 64 62 59 58 57 42 PP3V3_S5

13 IN EDP_PANEL_PWR

CRITICAL

U8300

FPF1009

MFET 2X2 8IN

1 ON

2 VIN_1 VOUT_1 4

3 VIN_2 VOUT_2 5

GND 6 THRM PAD 7

PP3V3_S0SW_LCD_R — Sense resistor on sensor page — 43 PP3V3_S0SW_LCD

L8304 FERR-120-OHM-1.5A 0402 LF

64 PP3V3_S0SW_LCD_UF

MIN LINE WIDTH=0.30 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V

C8315 1000PF 10% 16V X7R 1 0201

C8309 0.1UF 10% 6.3V CERM X5R 0201

C8311 0.1UF 10% 6.3V CERM X5R 0201

C8312 10UF 20% 6.3V X5R 603

C8324 0.1UF 10% 16V X5R CERM 0201

C8325 0.1UF 10% 16V X5R CERM 0201

C8320 0.1UF 10% 16V X5R CERM 0201

C8321 0.1UF 10% 16V X5R CERM 0201

67 5 BI DP_INT_AUXCH_C_N — (DP_INT_AUX_CH_C_N)

67 5 BI DP_INT_AUXCH_C_P — (DP_INT_AUX_CH_C_P)

67 5 IN DP_INT_ML_C_P<0>

67 5 IN DP_INT_ML_C_N<0>

67 64 DP_INT_AUX_CH_C_N

67 64 DP_INT_AUX_CH_C_P

67 64 DP_INT_ML_P<0>

67 64 DP_INT_ML_N<0>

PLACE NEAR=J8300.24 1mm

PLACE NEAR=J8300.25 1mm

R8318 1M 5% 1/20W MF 201

R8317 1M 5% 1/20W MF 201

PLACE NEAR=J8300.14 2mm

R8350 100K 5% 1/20W MF 201

R8380 1M 5% 1/20W MF 201

R8370 1M 5% 1/20W MF 201

PLACE NEAR=J8300.3 2mm

C8317 1000PF 5% 50V C0G CERM 603

SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE: Internal DisplayPort Connector

Apple Inc.

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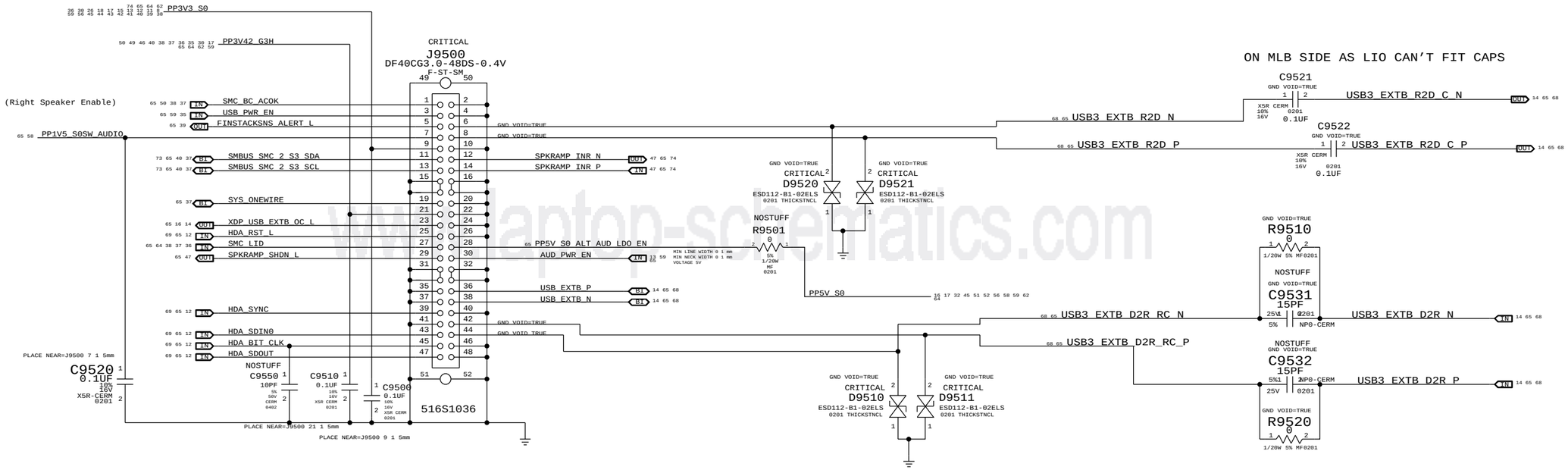

IO Ports

SYNC_MASTER=CLEAN_J43	SYNC_DATE=11/13/2012
PAGE TITLE	Left I/O (LIO) Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPBUS_G3H — MIN LINE WIDTH 0 6 mm; MIN NECK WIDTH 0 25 mm; VOLTAGE 8 6V; MAKE BASE TRUE
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS — MIN LINE WIDTH 0 6 mm; MIN NECK WIDTH 0 25 mm; VOLTAGE 8 6V; MAKE BASE TRUE
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_OTHER_ISNS
PPBUS_S5_HS_OTHER_ISNS — MIN LINE WIDTH 0 6 mm; MIN NECK WIDTH 0 25 mm; VOLTAGE 8 6V; MAKE BASE TRUE
PPBUS_S5_HS_OTHER_ISNS
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 25 MM; VOLTAGE 18 5V; MAKE BASE TRUE
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL
PPDCIN_G3H
PPDCIN_G3H — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 25 MM; VOLTAGE 18 5V; MAKE BASE TRUE
PPDCIN_G3H
PP3V42_G3H
PP3V42_G3H — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 3 42V; MAKE BASE TRUE
PP3V42_G3H ×16
PPVRTC_G3H
PPVRTC_G3H — MIN LINE WIDTH 0 2 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 3V; MAKE BASE TRUE
PPVRTC_G3H

5V Rails

PP5V_S5
PP5V_S5 — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 5V; MAKE BASE TRUE
PP5V_S5
PP5V_S5
PP5V_S4RS3
PP5V_S4RS3 — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 175 MM; VOLTAGE 5V; MAKE BASE TRUE
PP5V_S4RS3 ×4
PP5V_S0
PP5V_S0 — MIN LINE WIDTH 0 5 mm; MIN NECK WIDTH 0 2 mm; VOLTAGE 5V; MAKE BASE TRUE
PP5V_S0 ×10

3.3V Rails

PP3V3_S5
PP3V3_S5 — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S5 ×30
PP3V3_S4
PP3V3_S4 — MIN LINE WIDTH 0 60MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S4 ×6
PP3V3_SUS
PP3V3_SUS — MIN LINE WIDTH 0 50MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_SUS ×12
PP3V3_S3
PP3V3_S3 — MIN LINE WIDTH 0 50MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S3 ×12
PP3V3_S0
PP3V3_S0 — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S0 ×30
PP3V3_S45W_SNS
PP3V3_S45W_SNS — MIN LINE WIDTH 0 50MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S45W_SNS ×20

PP3V3_S05SW_SSD
PP3V3_S05SW_SSD — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 20MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_S05SW_SSD
PP3V3_S4_TBTAPWR
PP3V3_S4_TBTAPWR — MIN LINE WIDTH 0 38 MM; MIN NECK WIDTH 0 20 MM; VOLTAGE 3 3V; MAKE BASE TRUE

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3 — 2A max supply
PP1V8_S3 — MIN LINE WIDTH 0 6MM; MIN NECK WIDTH 0 2MM; VOLTAGE 1 2V; MAKE BASE TRUE
PP1V8_S3
PP1V8_S3
PP1V2_S3
PP1V2_S3 — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 1 MM; VOLTAGE 1 2V; MAKE BASE TRUE
PP1V2_S3 ×12
PP1V05_SUS
PP1V05_SUS — MIN LINE WIDTH 0 4 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 1 05V; MAKE BASE TRUE
PP1V05_SUS
PP1V5_S0
PP1V5_S0 — MIN LINE WIDTH 0 3 mm; MIN NECK WIDTH 0 17 mm; VOLTAGE 1 5V; MAKE BASE TRUE
PP1V5_S0 ×4
PP0V6_S0_DDRVTT
PP0V6_S0_DDRVTT — MIN LINE WIDTH 0 6 mm; MIN NECK WIDTH 0 17 mm; VOLTAGE 0 75V; MAKE BASE TRUE
PP0V6_S0_DDRVTT ×3
PP1V05_S0
PP1V05_S0 — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 175 MM; VOLTAGE 1 05V; MAKE BASE TRUE
PP1V05_S0 ×16
PP1V05_S0SW_PCH_HSIO
PP1V05_S0SW_PCH_HSIO — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 1 05V; MAKE BASE TRUE
PP1V05_S0SW_PCH_HSIO ×2

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
PPHV_S0SW_LCDBKLT — MIN LINE WIDTH 0 5 MM; MIN NECK WIDTH 0 375 MM; VOLTAGE 56V; MAKE BASE TRUE
PPHV_S0SW_LCDBKLT

TBT Rails (off when no cable)

PP15V_TBT
PP15V_TBT — MIN LINE WIDTH 0 4 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 17 8V; MAKE BASE TRUE
PP15V_TBT
PP3V3_TBTLC
PP3V3_TBTLC — MIN LINE WIDTH 0 4 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 3 3V; MAKE BASE TRUE
PP3V3_TBTLC ×2
PP1V05_TBTCIO
PP1V05_TBTCIO — MIN LINE WIDTH 0 4 MM; MIN NECK WIDTH 0 2 MM; VOLTAGE 1 05V; MAKE BASE TRUE
PPVIN_SW_TBTBST
PPVIN_SW_TBTBST — VOLTAGE 12 8V

CPU "VCORE" RAILS

PPVCC_S0_CPU
PPVCC_S0_CPU — MIN LINE WIDTH 0 6 MM; MIN NECK WIDTH 0 25 MM; VOLTAGE 1 8V; MAKE BASE TRUE
PPVCC_S0_CPU ×2

Digital Ground

GND — VOLTAGE=0V; MIN NECK WIDTH=0 075MM; MIN LINE WIDTH=0 6MM

SYNC_MASTER=WILL_J43 — SYNC_DATE=12/17/2012
PAGE TITLE: Power Aliases
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LPDDR3 Command/Address

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	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	20 24 70
	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	20 24 70
	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	20 24 70
	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	20 24 70
70 63 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 63 70
	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	20 24 70
	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	20 24 70
	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	20 24 70
	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	21 24 70
	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	21 24 70
	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	21 24 70
	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	21 24 70
	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	21 24 70
	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	21 24 70
70 63 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 63 70
	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	21 24 70
	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	21 24 70
	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	21 24 70
70 63 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 63 70
63 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 63
63 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 63
	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	22 24 70
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70 63 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 63 70
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	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	23 24 70
	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	23 24 70
	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	23 24 70
	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	23 24 70
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70 63 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 63 70
	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	23 24 70
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70 63 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 63 70
63 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 63
63 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 63

Memory Bit/Byte Swizzle

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70 63 21 7	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	7 21 63 70
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70 63 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	7 21 63 70
70 63 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	7 21 63 70
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70 63 23 7	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	7 23 63 70
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70 63 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 63 70
70 63 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 63 70

SYNC_MASTER=J41_MLB SYNC_DATE=08/30/2012

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Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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Functional Test Points

J3501: AirPort / BT Connector

FUNC TEST

TRUE	PP3V3_WLAN (Need 6 TPs)	29 37 38 39 41
TRUE	WIFI_EVENT_L	29 37 38
TRUE	PCIE_AP_R2D_N	29 69
TRUE	PCIE_AP_R2D_P	29 69
TRUE	PCIE_CLK100M_AP_N	12 29 69
TRUE	PCIE_CLK100M_AP_P	12 29 69
TRUE	PCIE_AP_D2R_P	14 29 69
TRUE	PCIE_AP_D2R_N	14 29 69
TRUE	PCIE_WAKE_L	13 29 31
TRUE	AP_RESET_CONN_L	29
TRUE	AP_CLKREQ_O_L	29
TRUE	USB_BT_CONN_P	29 68
TRUE	USB_BT_CONN_N	29 68
TRUE	PP3V3_S4	25 26 27 29 33 36 38 39 58 62 64

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC TEST

TRUE	PP3V3_S0SW_SSD_FLT (Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>	30 67
TRUE	PCIE_SSD_R2D_P<3..0>	30 67
TRUE	PP3V3_S0	42 43 44 45 56 59 61 62 64 65 74
TRUE	SSD_RESET_CONN_L	30
TRUE	SSD_CLKREQ_CONN_L	30
TRUE	SMC_OOB1_R2D_CONN_L	30
TRUE	SMC_OOB1_D2R_CONN_L	30
TRUE	SSD_PCIE_SEL_L	30
TRUE	SSD_SR_EN_L	15 30
TRUE	SMC_PWRFAIL_WARN_L	30 37
TRUE	SSD_PWR_EN	15 30 58 59
TRUE	PCIE_SSD_D2R_N<3..0>	12 30 67
TRUE	PCIE_SSD_D2R_P<3..0>	12 30 67
TRUE	PCIE_CLK100M_SSD_N	12 30 67
TRUE	PCIE_CLK100M_SSD_P	12 30 67

(Need to add 6 GND TPS)

J4002: Camera Connector

FUNC TEST

TRUE	MIPI_CLK_CONN_N	32 72
TRUE	MIPI_CLK_CONN_P	32 72
TRUE	CAM_SENSOR_WAKE_L_CONN	32
TRUE	MIPI_DATA_CONN_N	32 72
TRUE	MIPI_DATA_CONN_P	32 72
TRUE	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 69 73
TRUE	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 69 73
TRUE	I2C_CAM_SCK	31 32
TRUE	I2C_CAM_SDA	31 32
TRUE	PP5V_S3RS0_ALSCAM_F (Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC TEST

TRUE	SPI_ALT_IO2_WP_L	46
TRUE	SPI_ALT_IO3_HOLD_L	46
TRUE	LPC_AD<3..0>	14 37 69
TRUE	SPI_ALT_IO0_MOSI	46
TRUE	XDP_LPCPLUS_GPIO	15 16
TRUE	LPCPLUS_RESET_L	69
TRUE	SMC_TDO	37 38
TRUE	TP_SMC_TRST_L	
TRUE	TP_SMC_MD1	
TRUE	SMC_TX_L	37 38
TRUE	SPI_ALT_IO1_MISO	46
TRUE	LPC_FRAME_L	14 37 69
TRUE	SPIROM_USE_MLB	15 46
TRUE	PM_CLKRUN_L	13 37
TRUE	SPI_ALT_CLK	46
TRUE	SPI_ALT_CS_L	46
TRUE	LPC_SERIRQ	15 37
TRUE	LPC_PWRDWN_L	13 37
TRUE	SMC_TDI	37 38
TRUE	SMC_TCK	37 38 46
TRUE	SMC_RESET_L	37 38 46 50
TRUE	SMC_ROMBOOT	
TRUE	SMC_RX_L	37 38
TRUE	SMC_TMS	37 38 46

(Need to add 6 GND TPs)

TRUE	GND	

J6000: Fan Connector

FUNC TEST

TRUE	PP5V_S0	16 17 32 45 51 52 56 58 59 61 62
TRUE	FAN_RT_TACH	45
TRUE	FAN_RT_PWM	45

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC TEST

TRUE	SMC_LID	36 37 38 61 65
TRUE	TPAD_SPI_MISO_R	36
TRUE	USB_TPAD_P	14 36 68
TRUE	USB_TPAD_N	14 36 68
TRUE	TPAD_SPI_CLK_R	36
TRUE	TPAD_WAKE_L	36
TRUE	TPAD_SPI_MOSI_R	36
TRUE	PP3V3_S4_IPD	36
TRUE	TPAD_SPI_CS_R_L	36
TRUE	TPAD_SPI_IF_EN_CONN	36
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN	36
TRUE	PP5V_S4_IPD	36
TRUE	TPAD_USB_IF_EN_CONN	36
TRUE	SMBUS_SMC_3_SDA	36 37 40 44 73
TRUE	SMBUS_SMC_3_SCL	36 37 40 44 73
TRUE	SMC_LSOC_RST_L	36 38
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	SMC_ONOFF_L	36 37 38

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC TEST

TRUE	PPDCIN_G3H (Need 4 TPs)	49 50 62 64
TRUE	PP5V_S4RS3 (Need 3 TPs)	32 35 47 49 54 55 58 62

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC TEST

TRUE	SPKRAMP_ROUT_P	47 74
TRUE	SPKRAMP_ROUT_N	47 74

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC TEST

TRUE	PPVBAT_G3H_CONN (Need 4 TPs)	48 50
TRUE	SMBUS_SMC_5_G3_SCL	37 40 48 50 73
TRUE	SMBUS_SMC_5_G3_SDA	37 40 48 50 73
TRUE	SYS_DETECT_L	48

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC TEST

TRUE	PPHV_S0SW_LCDBKLT (Need 2 TPs)	56 60 62
TRUE	LED_RETURN_6	56 60
TRUE	LED_RETURN_5	56 60
TRUE	LED_RETURN_4	56 60
TRUE	LED_RETURN_3	56 60
TRUE	LED_RETURN_2	56 60
TRUE	LED_RETURN_1	56 60
TRUE	DP_INT_HPD_CONN	60
TRUE	I2C_TCON_SDA_R	60
TRUE	I2C_TCON_SCL_R (Need 2 TPs)	60
TRUE	PP3V3_S0SW_LCD_UF	60
TRUE	DP_INT_AUX_CH_C_N	60 67
TRUE	DP_INT_AUX_CH_C_P	60 67
TRUE	DP_INT_ML_P<0>	60 67
TRUE	DP_INT_ML_N<0>	60 67

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC TEST

TRUE	KBDLED_ANODE	56
TRUE	KBDLED_FB	56

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC TEST

776	TRUE	XDP_CPU_TCK	6 16 67
777	TRUE	XDP_PCH_TCK	12 16 69
778	TRUE	XDP_CPU_TDI	6 16 67
779	TRUE	XDP_CPU_TDO	6 16 67
780	TRUE	XDP_CPUPCH_TRST_L	6 12 16 67
781	TRUE	XDP_CPU_TMS	6 16 67
782	TRUE	XDP_PCH_TMS	12 16 69
783	TRUE	XDP_PCH_TDI	12 16 69
784	TRUE	XDP_PCH_TDO	12 16 69
785	TRUE	XDP_CPU_PREQ_L	6 16 67
786	TRUE	XDP_CPU_PRDY_L	6 16 67
787	TRUE	XDP_CPU_VCCST_PWRGD	16
788	TRUE	PM_RSMRST_L	13 59
789	TRUE	XDP_SYS_PWROK	16
790	TRUE	PM_SYSRST_L	13 17 37
791	TRUE	CPU_CFG<3>	6 16 67
792	TRUE	PP1V05_S0	6 9 11 15 16 17 38 42 51 55 58 59 62 64

(Need to add 2 GND TPs)

Misc Voltages & Control Signals

FUNC TEST

TRUE	PPBUS_G3H	27 41 42 49 50 56 62
TRUE	PPVIN_SW_TBTBST	62
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	41 51 52 53 55 62
TRUE	PPDCIN_G3H	49 50 62 64
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	PPVRTC_G3H	8 12 13 17 62
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 74
TRUE	PP3V3_SUS	8 11 14 18 46 57 58 59 62
TRUE	PP3V3_S3	15 18 19 33 36 40 41 58 62
TRUE	PP3V3_S0	62 64 65 74
TRUE	PP3V3_S0SW_SSD	8 11 12 13 15 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61
TRUE	PP1V5_S0	30 41 62
TRUE	PP1V05_S0	8 57 58 59 62
TRUE	PP15V_TBT	6 8 11 15 16 17 38 42 51 55 58 59 62 64
TRUE	PP3V3_TBTLC	27 28 62
TRUE	PP1V05_TBT	17 18 25 26 62
TRUE	PPVCC_S0_CPU	26
TRUE	PP1V05_TBTCIO	8 10 42 52 62
TRUE	PPBUS_S5_HS_OTHER_ISNS	26 62
TRUE	PPDCIN_G3H_ISOL	41 54 62
TRUE	PP3V3_S4	42 49 50 62

(Need to add 27 GND TPs)

TRUE	PP3V3_S4	25 26 27 29 33 36 38 39 58 62 64

NO_TEST Nets

NO TEST — MAKE BASE

64	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	64
64	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	64
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 64
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 64
64 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 64
64 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 64
64 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 64
64 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 64
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 64
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 64
64 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 64
64 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 64
64 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 64
64 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 64
67	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5
67	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5
64 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 64
64 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 64
64 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 64
64 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 64
64 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 64

CPU/PCH

64 37	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	37 64
64	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	64
64	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	64
64	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	64
64 37	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	37 64
64 37	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	37 64
64 37	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	37 64
64 37	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	37 64
64 37	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	37 64
64	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	64
64	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	64
64	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	64
64 37	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	37 64
64 37	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	37 64
64 37	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	37 64
64 37	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	37 64
64 37	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	37 64

SMC

71	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25
71	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25
71	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25
71	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25
64 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 64
71 64	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	64 71
71 64	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	64 71
71 64 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 64 71
71 64 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 64 71
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>	
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>	
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>	
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>	
64 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 64
64 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 64
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>	
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>	
64 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 64
64 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 64

TBT

Unused nets with offpage

(Nets with offpages not used on this project)

PCH_BT_UART_D2R	15	
PCH_BT_UART_R2D	15	
PCH_BT_UART_RTS_L	15	
PCH_BT_UART_CTS_L	15	
AUD_SPI_CS_L	15	
AUD_SPI_CLK	15	
AUD_SPI_MISO	15	
AUD_SPI_MOSI	15	
HDMITBTMUX_LATCH	13	
HDD_PWR_EN	15	
WOL_EN	14	
BT_PWRRST_L	15	
HDMITBTMUX_FLAG	13	
FW_PWR_EN		
FW_PME_L		
ENET_MEDIA_SENSE	15	
LCD_PSR_EN	15	
LCD_IRQ_L	15	
ODD_PWR_EN_L	13	
ENET_LOW_PWR	13	
AUD_IP_PERIPHERAL_DET		
AUD_I2C_INT_L		
AP_PCIE_DEV_WAKE	13	

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: Func Test / No Test

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Functional Test Points

J9500: LIO Connector

FUNC TEST		
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50
TRUE	PP3V3_S0	62 64 74 59 61 68
TRUE	PP1V5_S0SW_AUDIO	9 11 12 13 15 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61
TRUE	SYS_ONEWIRE	37 61
TRUE	SMC_BC_ACOK	37 38 50 61
TRUE	USB_PWR_EN	35 59 61
TRUE	SMBUS_SMC_2_S3_SDA	37 40 61 73
TRUE	SMBUS_SMC_2_S3_SCL	37 40 61 73
TRUE	SPKRAMP_SHDN_L	47 61
TRUE	FINSTACKSNS_ALERT_L	39 61
TRUE	SPKRAMP_INR_N	47 61 74
TRUE	SPKRAMP_INR_P	47 61 74
TRUE	USB_EXTB_N	14 61 68
TRUE	USB_EXTB_P	14 61 68
TRUE	PP5V_S0_ALT_AUD_LDO_EN	61
TRUE	SMC_LID	36 37 38 61 64
TRUE	HDA_SDOUT	12 61 69
TRUE	HDA_BIT_CLK	12 61 69
TRUE	HDA_SDIN0	12 61 69
TRUE	XDP_USB_EXTB_OC_L	14 16 61
TRUE	HDA_RST_L	12 61 69
TRUE	HDA_SYNC	12 61 69
TRUE	USB3_EXTB_D2R_RC_P	61 65 68
TRUE	USB3_EXTB_D2R_RC_N	61 65 68
TRUE	USB3_EXTB_R2D_P	61 65 68
TRUE	USB3_EXTB_R2D_N	61 65 68
TRUE	AUD_PWR_EN	13 59 61

(Need to add 5 GND TPs)

SD Card Aliases

		MAKE BASE		
68 65 34 14	USB3_SD_D2R_P	TRUE	USB3_SD_D2R_P	14 34 65 68
68 65 34 14	USB3_SD_D2R_N	TRUE	USB3_SD_D2R_N	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_P	TRUE	USB3_SD_R2D_C_P	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_N	TRUE	USB3_SD_R2D_C_N	14 34 65 68
65 39 37 34 15	PP3V3_S0SW_SD		PP3V3_S0SW_SD	15 34 37 39 65

(MAKE_BASE=TRUE on page 45)

Bead Probes

68 61 14	USB3_EXTB_D2R_N	BEAD-PROBE	BPA511
68 61 14	USB3_EXTB_D2R_P	BEAD-PROBE	BPA510
68 65 61	USB3_EXTB_D2R_RC_N	BEAD-PROBE	BPA520
68 65 61	USB3_EXTB_D2R_RC_P	BEAD-PROBE	BPA521
68 61 14	USB3_EXTB_R2D_C_N	BEAD-PROBE	BPA513
68 61 14	USB3_EXTB_R2D_C_P	BEAD-PROBE	BPA512
68 65 61	USB3_EXTB_R2D_N	BEAD-PROBE	BPA523
68 65 61	USB3_EXTB_R2D_P	BEAD-PROBE	BPA522

SYNC_MASTER=J41_MLB SYNC_DATE=09/13/2012

PAGE TITLE: Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 ISL8 ISL9 ISL10 ISL11 BOTTOM	NO TYPE BGA MEM TERM	MM	16 2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP BOTTOM	Y	=50 OHM SE	=50 OHM SE			
DEFAULT	ISL2 ISL11	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	ISL3 ISL10	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	ISL4 ISL9	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4 OHM SE	TOP BOTTOM	Y	0 310 MM	0 310 MM			
27P4 OHM SE	ISL2 ISL11	Y	0 182 MM	0 182 MM			
27P4 OHM SE	ISL3 ISL10	Y	0 182 MM	0 182 MM			
27P4 OHM SE	ISL4 ISL9	Y	0 182 MM	0 182 MM			
27P4 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35 OHM SE	TOP BOTTOM	Y	0 195 MM	0 195 MM			
35 OHM SE	ISL2 ISL11	Y	0 125 MM	0 125 MM			
35 OHM SE	ISL3 ISL10	Y	0 125 MM	0 125 MM			
35 OHM SE	ISL4 ISL9	Y	0 125 MM	0 125 MM			
35 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40 OHM SE	TOP BOTTOM	Y	0 170 MM	0 170 MM			
40 OHM SE	ISL2 ISL11	Y	0 096 MM	0 096 MM			
40 OHM SE	ISL3 ISL10	Y	0 096 MM	0 096 MM			
40 OHM SE	ISL4 ISL9	Y	0 099 MM	0 099 MM			
40 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45 OHM SE	TOP BOTTOM	Y	0 135 MM	0 135 MM			
45 OHM SE	ISL2 ISL11	Y	0 075 MM	0 075 MM			
45 OHM SE	ISL3 ISL10	Y	0 075 MM	0 075 MM			
45 OHM SE	ISL4 ISL9	Y	0 080 MM	0 080 MM			
45 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50 OHM SE	TOP BOTTOM	Y	0 110 MM	0 110 MM			
50 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55 OHM SE	TOP BOTTOM	Y	0 090 MM	0 090 MM			
55 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 165 MM		0 110 MM	0 110 MM
70 OHM DIFF	ISL2 ISL11	Y	0 105 MM	0 105 MM		0 100 MM	0 100 MM
70 OHM DIFF	ISL3 ISL10	Y	0 105 MM	0 105 MM		0 100 MM	0 100 MM
70 OHM DIFF	ISL4 ISL9	Y	0 110 MM	0 110MM		0 095 MM	0 095 MM
70 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80 OHM DIFF	TOP BOTTOM	Y	0 132 MM	0 132 MM		0 130 MM	0 130 MM
80 OHM DIFF	ISL2 ISL11	Y	0 081 MM	0 081 MM		0 115 MM	0 115 MM
80 OHM DIFF	ISL3 ISL10	Y	0 081 MM	0 081 MM		0 115 MM	0 115 MM
80 OHM DIFF	ISL4 ISL9	Y	0 088 MM	0 088 MM		0 110 MM	0 110 MM
80 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	TOP BOTTOM	Y	0 115 MM	0 115 MM		0 200 MM	0 200 MM
90 OHM DIFF	ISL2 ISL11	Y	0 070 MM	0 070 MM		0 180 MM	0 180 MM
90 OHM DIFF	ISL3 ISL10	Y	0 070 MM	0 070 MM		0 180 MM	0 180 MM
90 OHM DIFF	ISL4 ISL9	Y	0 076 MM	0 076 MM		0 180 MM	0 180 MM
90 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1 1 SPACING	*	0 100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x DIELECTRIC	TOP BOTTOM	0 071 MM	?
1x DIELECTRIC	ISL3 ISL10	0 053 MM	?
1x DIELECTRIC	ISL4 ISL9	0 050 MM	?
1x DIELECTRIC	*	0 090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 165 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL2 ISL11	Y	0 106 MM	0 106 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL3 ISL10	Y	0 106 MM	0 106 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL4 ISL9	Y	0 110 MM	0 110 MM		0 150 MM	0 150 MM
73 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	TOP BOTTOM	Y	0 120 MM	0 120 MM		0 150 MM	0 150 MM
85 OHM DIFF	ISL2 ISL11	Y	0 078 MM	0 078 MM		0 160 MM	0 160 MM
85 OHM DIFF	ISL3 ISL10	Y	0 078 MM	0 078 MM		0 160 MM	0 160 MM
85 OHM DIFF	ISL4 ISL9	Y	0 082 MM	0 082 MM		0 140 MM	0 140 MM
85 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC MASTER=CONSTRAINTS SYNC_DATE=10/24/2012

PAGE TITLE: PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CPU 27P4S	*	27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	0 100 MM	0 100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	TOP BOTTOM	=2x DIELECTRIC	?
CPU AGTL	*	=STANDARD	?

Note CPU 8MIL and CPU ITP can be converted back to TABLE SPACING RULE once rdar //10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU 8MIL	*	*	CPU 8MIL 2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU 8MIL 2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU ITP	*	*	CPU ITP 2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU ITP 2ANY	*	=4x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	CPU COMP	*	CPU COMP 2SELF
CPU COMP	*	*	CPU COMP 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU COMP 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CPU COMP 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU COMP 2SELF	*	=4x DIELECTRIC	?
CPU COMP 2OTHER	*	=6x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU VCCSENSE	CPU VCCSENSE	*	CPU VCCSENSE 2SELF
CPU VCCSENSE	*	*	CPU VCCSENSE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU VCCSENSE 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CPU VCCSENSE 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU VCCSENSE 2SELF	*	=4x DIELECTRIC	?
CPU VCCSENSE 2OTHER	*	=6x DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF
CLK PCIE 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK PCIE	CLK PCIE	*	CLK PCIE 2SELF
CLK PCIE	*	*	CLK PCIE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCIE 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CLK PCIE 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCIE 2SELF	*	=4x DIELECTRIC	?
CLK PCIE 2OTHER	*	=6x DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE CPU TX	PCIE CPU TX	*	PCIE TX2TX
PCIE CPU RX	PCIE CPU RX	*	PCIE RX2RX
PCIE CPU TX	* CPU TX	*	PCIE TX2OTHERTX
PCIE CPU RX	* CPU RX	*	PCIE RX2OTHERRX
PCIE CPU TX	* CPU RX	*	PCIE TX2RX
PCIE CPU RX	* CPU TX	*	PCIE RX2TX
PCIE CPU TX	* TX	*	PCIE 2OTHERHS
PCIE CPU RX	* TX	*	PCIE 2OTHERHS
PCIE CPU TX	* RX	*	PCIE 2OTHERHS
PCIE CPU RX	* RX	*	PCIE 2OTHERHS
PCIE CPU TX	*	*	PCIE 2OTHER
PCIE CPU RX	*	*	PCIE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE TX2TX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE RX2RX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE TX2OTHERTX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE RX2OTHERRX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE TX2RX	TOP BOTTOM	=7x DIELECTRIC	?
PCIE RX2TX	TOP BOTTOM	=7x DIELECTRIC	?
PCIE 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
PCIE 2OTHER	TOP BOTTOM	=5x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE TX2TX	*	=2 5x DIELECTRIC	?
PCIE RX2RX	*	=2 5x DIELECTRIC	?
PCIE TX2OTHERTX	*	=4x DIELECTRIC	?
PCIE RX2OTHERRX	*	=4x DIELECTRIC	?
PCIE TX2RX	*	=6x DIELECTRIC	?
PCIE RX2TX	*	=6x DIELECTRIC	?
PCIE 2OTHERHS	*	=4x DIELECTRIC	?
PCIE 2OTHER	*	=3x DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE PCH TX	PCIE PCH TX	*	PCIE TX2TX
PCIE PCH RX	PCIE PCH RX	*	PCIE RX2RX
PCIE PCH TX	* PCH TX	*	PCIE TX2OTHERTX
PCIE PCH RX	* PCH RX	*	PCIE RX2OTHERRX
PCIE PCH TX	* PCH RX	*	PCIE TX2RX
PCIE PCH RX	* PCH TX	*	PCIE RX2TX
PCIE PCH TX	* TX	*	PCIE 2OTHERHS
PCIE PCH RX	* TX	*	PCIE 2OTHERHS
PCIE PCH TX	* RX	*	PCIE 2OTHERHS
PCIE PCH RX	* RX	*	PCIE 2OTHERHS
PCIE PCH TX	*	*	PCIE 2OTHER
PCIE PCH RX	*	*	PCIE 2OTHER

SOURCE 471984 Chief River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
CPU_PECI	CPU 45S	CPU COMP	CPU_PECI	6 38
PM_SYNC	CPU 45S	CPU AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU 45S	CPU AGTL	PM_MEM_PWRGD	
	CPU 45S	CPU ITP	XDP_DBRESET_L	16 17
	CPU 45S	CPU ITP	XDP_CPU_PRDY_L	6 16 64
	CPU 45S	CPU ITP	XDP_CPU_PREQ_L	6 16 64
	CPU 27P4S	CPU COMP	EDP_COMP	
	CPU 27P4S	CPU COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<2>	6
	CPU 45S	CPU ITP	CPU_CFG<11..0>	6 16 64
CPU_CATERR_L	CPU 45S	CPU AGTL	CPU_CATERR_L	6 37
	CPU 45S	CPU AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU 45S	CPU AGTL	CPU_PROCHOT_L	6 37 38 51
CPU_PWRGD	CPU 45S	CPU AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU 45S	CPU RMTL	PM_THRMTRIP_L	15 38
DMI_CLK100M	CLK PCIE 80D	CLK PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK PCIE 80D	CLK PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK PCIE 80D	CLK PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK PCIE 80D	CLK PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU 45S	CPU ITP	XDP_CPU_TDI	6 16 64
XDP_TDO	CPU 45S	CPU ITP	XDP_CPU_TDO	6 16 64
XDP_TMS	CPU 45S	CPU ITP	XDP_CPU_TMS	6 16 64
XDP_TCK	CPU 45S	CPU ITP	XDP_CPU_TCK	6 16 64
XDP_TRST_L	CPU 45S	CPU ITP	XDP_CPUPCH_TRST_L	6 12 16 64
XDP_BPM_L	CPU 45S	CPU ITP	XDP_BPM_L<1..0>	6 16
	CPU 45S	CPU ITP	XDP_BPM_L<7..2>	6 16
	CPU 45S	CPU ITP	XDP_OBSDATA_B<3..0>	
	CPU 45S	CPU ITP	CPU_CFG<15..12>	6 16
(ESB_CPURST_L)	CPU 45S	CPU ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 51
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 51
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 51
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 51
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 51
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 64
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	60 64
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 60 64
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 60
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 60
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE: CPU Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA ICOMP	*	=4x DIELECTRIC	?

SOURCE 471984 Chief River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=4x DIELECTRIC	?

SOURCE Calpella Platform Design Guide for Ibex Peak M (DG 398905 398905 v1 5) Section 3 8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3 PCH TX	USB3 PCH TX	*	USB3 TX2TX
USB3 PCH RX	USB3 PCH RX	*	USB3 RX2RX
USB3 PCH TX	* PCH TX	*	USB3 TX2OTHERTX
USB3 PCH RX	* PCH RX	*	USB3 RX2OTHERRX
USB3 PCH TX	* PCH RX	*	USB3 TX2RX
USB3 PCH RX	* PCH TX	*	USB3 RX2TX
USB3 PCH TX	* TX	*	USB3 2OTHERHS
USB3 PCH RX	* TX	*	USB3 2OTHERHS
USB3 PCH TX	* RX	*	USB3 2OTHERHS
USB3 PCH RX	* RX	*	USB3 2OTHERHS
USB3 PCH TX	*	*	USB3 2OTHER
USB3 PCH RX	*	*	USB3 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 TX2TX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 RX2RX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 TX2OTHERTX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 RX2OTHERRX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 TX2RX	TOP BOTTOM	=7x DIELECTRIC	?
USB3 RX2TX	TOP BOTTOM	=7x DIELECTRIC	?
USB3 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
USB3 2OTHER	TOP BOTTOM	=5x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 TX2TX	*	=2 5x DIELECTRIC	?
USB3 RX2RX	*	=2 5x DIELECTRIC	?
USB3 TX2OTHERTX	*	=4x DIELECTRIC	?
USB3 RX2OTHERRX	*	=4x DIELECTRIC	?
USB3 TX2RX	*	=6x DIELECTRIC	?
USB3 RX2TX	*	=6x DIELECTRIC	?
USB3 2OTHERHS	*	=4x DIELECTRIC	?
USB3 2OTHER	*	=3x DIELECTRIC	?

SOURCE 471984 Cheif River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 64
	USB_80D	USB	USB_BT_CONN_N	29 64
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 36 64
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 36 64
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 36
	SPI_45S	SPI	TPAD_SPI_MISO	15 36
	SPI_45S	SPI	TPAD_SPI_CLK	15 36
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 35
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 35
	UART_45S	UART	SMC_DEBUGPRT_TX_L	35 37 38
	UART_45S	UART	SMC_DEBUGPRT_RX_L	35 37 38
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	35
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 35
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 35
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 61 65
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 61 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_P	14 34 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_N	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_P	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_N	14 34 65
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	34
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	34
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PAGE TITLE: PCH Constraints 1

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x DIELECTRIC	?
CLK LPC	*	=4x DIELECTRIC	?

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 45S R 50S	TOP BOTTOM	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE		
SMB 45S R 50S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

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SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	=4x DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH ITP	*	=2 1 SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2DP	*	=3x DIELECTRIC	?
DP 2OTHERHS	*	=4x DIELECTRIC	?
DP 2OTHER	*	=3x DIELECTRIC	?
DP AUX	*	=3x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2DP	TOP BOTTOM	=4x DIELECTRIC	?
DP 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
DP 2OTHER	TOP BOTTOM	=4x DIELECTRIC	?
DP AUX	TOP BOTTOM	=4x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP TX	DP TX	*	DP 2DP
DP TX	* TX	*	DP 2OTHERHS
DP TX	* RX	*	DP 2OTHERHS
DP TX	*	*	DP 2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK 25M 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	=2x DIELECTRIC	?
CLK 25M	*	=5x DIELECTRIC	?

NOTE 25MHz system clocks very sensitive to noise

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LPC_AD	LPC 45S	LPC	LPC_AD<3..0>	14 37 64
LPC_FRAME_L	LPC 45S	LPC	LPC_FRAME_L	14 37 64
	LPC 45S	LPC	LPCPLUS_RESET_L	64
LPC_CLK33M	CLK LPC 45S	CLK LPC	LPC_CLK24M_SMC	17 37
	CLK LPC 45S	CLK LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK LPC 45S	CLK LPC	LPC_CLK24M_LPCPLUS	
	CLK LPC 45S	CLK LPC	LPC_CLK24M_LPCPLUS_R	
SMBUS_PCH_CLK	SMB 45S R 50S	SMB	SMBUS_PCH_CLK	14 16 19 40 56
SMBUS_PCH_DATA	SMB 45S R 50S	SMB	SMBUS_PCH_DATA	14 16 19 40 56
SMBUS_PCH_0_CLK	SMB 45S R 50S	SMB	SML_PCH_0_CLK	14 40
SMBUS_PCH_0_DATA	SMB 45S R 50S	SMB	SML_PCH_0_DATA	14 40
SMBUS_SMC_1_S0_SCL	SMB 45S R 50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64 73
SMBUS_SMC_1_S0_SDA	SMB 45S R 50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64 73
HDA_BIT_CLK	HDA 45S	HDA	HDA_BIT_CLK	12 61 65
	HDA 45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA 45S	HDA	HDA_SYNC	12 61 65
	HDA 45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA 45S	HDA	HDA_RST_R_L	12
	HDA 45S	HDA	HDA_RST_L	12 61 65
HDA_SDIN0	HDA 45S	HDA	HDA_SDIN0	12 61 65
HDA_SDOUT	HDA 45S	HDA	HDA_SDOUT	12 61 65
	HDA 45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK SLOW 45S	CLK SLOW	PM_CLK32K_SUSCLK_R	13 38
	CLK SLOW 45S	CLK SLOW	SMC_CLK32K	37 38
SPI_CLK	SPI 45S	SPI	SPI_CLK_R	14 46
	SPI 45S	SPI	SPI_CLK	46
SPI_MOSI	SPI 45S	SPI	SPI_MOSI_R	14 46
	SPI 45S	SPI	SPI_MOSI	46
SPI_MISO	SPI 45S	SPI	SPI_MISO	14 46
	SPI 45S	SPI	SPI_MISO_R	46
SPI_CS0	SPI 45S	SPI	SPI_CS0_R_L	14 46
	SPI 45S	SPI	SPI_CS0_L	46
	SPI 45S	SPI	SPI_SMC_CLK	37 46
	SPI 45S	SPI	SPI_SMC_MOSI	37 46
	SPI 45S	SPI	SPI_SMC_MISO	37 46
	SPI 45S	SPI	SPI_SMC_CS_L	37 46
	SPI 45S	SPI	SPI_MLB_CLK	46
	SPI 45S	SPI	SPI_MLB_IO0_MOSI	46
	SPI 45S	SPI	SPI_MLB_IO1_MISO	46
	SPI 45S	SPI	SPI_MLB_CS_L	46
	SPI 45S	SPI	SPI_IO<2>	14 46
	SPI 45S	SPI	SPI_IO2_R	46
	SPI 45S	SPI	SPI_MLB_IO2_WP_L	46
	SPI 45S	SPI	SPI_IO<3>	14 46
	SPI 45S	SPI	SPI_IO3_R	46
	SPI 45S	SPI	SPI_MLB_IO3_HOLD_L	46
PCIE_AP_R2D	PCIE 80D	PCIE PCH TX	PCIE_AP_R2D_P	29 64
PCIE_AP_R2D	PCIE 80D	PCIE PCH TX	PCIE_AP_R2D_N	29 64
	PCIE 80D	PCIE PCH TX	PCIE_AP_R2D_C_P	14 29
	PCIE 80D	PCIE PCH TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE 80D	PCIE PCH RX	PCIE_AP_D2R_P	14 29 64
PCIE_AP_D2R	PCIE 80D	PCIE PCH RX	PCIE_AP_D2R_N	14 29 64
PCIE_CLK100M_AP	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_AP_P	12 29 64
PCIE_CLK100M_AP	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_AP_N	12 29 64
PCIE_TBT_R2D	PCIE 80D	PCIE PCH TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE 80D	PCIE PCH TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE 80D	PCIE PCH TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE 80D	PCIE PCH TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE 80D	PCIE PCH RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE 80D	PCIE PCH RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE 80D	PCIE PCH RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE 80D	PCIE PCH RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK PCIE 80D	CLK PCIE	PEG_CLK100M_P	
	CLK PCIE 80D	CLK PCIE	PEG_CLK100M_N	
XDP_TDI	PCH 45S	PCH ITP	XDP_PCH_TDI	12 16 64
XDP_TDO	PCH 45S	PCH ITP	XDP_PCH_TDO	12 16 64
XDP_TMS	PCH 45S	PCH ITP	XDP_PCH_TMS	12 16 64
XDP_TCK	PCH 45S	PCH ITP	XDP_PCH_TCK	12 16 64
PCIE_CAM	PCIE 80D	PCIE PCH TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE 80D	PCIE PCH TX	PCIE_CAMERA_R2D_N	31 32
	PCIE 80D	PCIE PCH TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE 80D	PCIE PCH TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE 80D	PCIE PCH RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE 80D	PCIE PCH RX	PCIE_CAMERA_D2R_N	14 32
	PCIE 80D	PCIE PCH RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE 80D	PCIE PCH RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK PCIE 80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SYSCLK_CLK32K_RTC	CLK SLOW 45S	CLK SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK 25M 45S	CLK 25M	CLK25M_CAM_CLKP	31 32
	CLK 25M 45S	CLK 25M	CLK25M_CAM_XTALP_R	32
	CLK 25M 45S	CLK 25M	CLK25M_CAM_XTALP	32
	CLK 25M 45S	CLK 25M	CLK25M_CAM_XTALN	32
	CLK 25M 45S	CLK 25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_TBT	17 25
	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_X1	17
	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_X2	17
	CLK 25M 45S	CLK 25M	SYSCLK_CLK25M_X2_R	17
	CLK 25M 45S	CLK 25M	SDCLK_CLK25M_X2	34
	CLK 25M 45S	CLK 25M	SDCLK_CLK25M_X2_R	34 75
	CLK 25M 45S	CLK 25M	SDSCLK_CLK25M_X1	34

SYNC_MASTER=J41_MLB SYNC_DATE=12/14/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40 OHM SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50 OHM SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70 OHM DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73 OHM DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM DATA2SELF	*	=2x_DIELECTRIC	?
MEM DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM CMD2CTRL	*	=3x_DIELECTRIC	?
MEM CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM 2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM 2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM 2OTHERMEM

Memory Net Properties

ELECTRICAL CONSTRAINT SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 63
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 63
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 63
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 63
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 63
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 63
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 63
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 63
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 63
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 63
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 63
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 63
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 63
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 63
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 63
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 63
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 63
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 63
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 63
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 63
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 63
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 63
		MEM_PWR	PP1V2_S3	17 19 20 21 22 23 42 53 62
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B	18 19 22 23
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B	18 19 22 23

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT SPI	*	=2x DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP 80D	*	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP TX	TBTDP TX	*	TBTDP TX2TX
TBTDP RX	TBTDP RX	*	TBTDP RX2RX
TBTDP TX	TBTDP RX	*	TBTDP TX2RX
TBTDP RX	TBTDP TX	*	TBTDP TX2RX
TBTDP TX	* TX	*	TBTDP 2OTHERHS
TBTDP RX	* TX	*	TBTDP 2OTHERHS
TBTDP TX	* RX	*	TBTDP 2OTHERHS
TBTDP RX	* RX	*	TBTDP 2OTHERHS
TBTDP TX	*	*	TBTDP 2OTHER
TBTDP RX	*	*	TBTDP 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP TX2TX	TOP BOTTOM	=6x DIELECTRIC	?
TBTDP RX2RX	TOP BOTTOM	=6x DIELECTRIC	?
TBTDP TX2RX	TOP BOTTOM	=10x DIELECTRIC	?
TBTDP 2OTHERHS	TOP BOTTOM	=10x DIELECTRIC	?
TBTDP 2OTHER	TOP BOTTOM	=6x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP TX2TX	*	=4x DIELECTRIC	?
TBTDP RX2RX	*	=4x DIELECTRIC	?
TBTDP TX2RX	*	=6x DIELECTRIC	?
TBTDP 2OTHERHS	*	=6x DIELECTRIC	?
TBTDP 2OTHER	*	=4x DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	64
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	64
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	64
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	64
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 64
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	*	4X DIELECTRIC	?
MIPI 2CLK	*	6X DIELECTRIC	?
MIPICLK 2OTHER	*	7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	TOP BOTTOM	6X DIELECTRIC	?
MIPI 2CLK	TOP BOTTOM	8X DIELECTRIC	?
MIPICLK 2OTHER	TOP BOTTOM	10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI DATA	*	*	MIPI 2OTHER
MIPI DATA	CLK MIPI	*	MIPI 2CLK
CLK MIPI	*	*	MIPICLK 2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2 MEM 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
S2 MEM 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2 DATA2SELF	*	=2x_DIELECTRIC	?
S2 DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2 CMD2CTRL	*	=2x_DIELECTRIC	?
S2 CTRL2CTRL	*	=2x_DIELECTRIC	?
S2 2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM 2PWR	*	=2x_DIELECTRIC	?
S2MEM 2GND	*	=2x_DIELECTRIC	?
S2MEM 2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2 DATA2SELF	TOP BOTTOM	=4x DIELECTRIC	?
S2 DQS2OWNDATA	TOP BOTTOM	=4x DIELECTRIC	?
S2_CMD2CMD	TOP BOTTOM	=4x DIELECTRIC	?
S2 CMD2CTRL	TOP BOTTOM	=4x DIELECTRIC	?
S2 CTRL2CTRL	TOP BOTTOM	=4x DIELECTRIC	?
S2 2OTHERMEM	TOP BOTTOM	=6x DIELECTRIC	?
S2MEM 2PWR	TOP BOTTOM	=4x DIELECTRIC	?
S2MEM 2GND	TOP BOTTOM	=4x DIELECTRIC	?
S2MEM 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2 MEM DATA*	*	*	S2MEM 2OTHER
S2 MEM DQS*	*	*	S2MEM 2OTHER
S2_MEM_CMD	*	*	S2MEM 2OTHER
S2_MEM_CTRL	*	*	S2MEM 2OTHER
S2_MEM_CLK	*	*	S2MEM 2OTHER
S2 MEM DATA*	=SAME	*	S2 DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2 CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2 CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2 2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2 MEM DATA1	*	S2 DQS2OWNDATA
S2_MEM_DQS0	S2 MEM DATA0	*	S2 DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 64
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 64
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 64
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1 DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0 1 MM	0 1 MM
2TO1 DIFFPAIR	*	=STANDARD	0 2 MM	0 1 MM	=STANDARD	0 1 MM	0 1 MM

SMC SMBus Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	37 40 60
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	37 40 60
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64 69
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64 69
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	37 40 61 65
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	37 40 61 65
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	36 37 40 44 64
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	36 37 40 44 64
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	37 40 48 50 64
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	37 40 48 50 64

SMBus Charger Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	50
	2TO1_DIFFPAIR		CHGR_CSI_R_P	50
	2TO1_DIFFPAIR		CHGR_CSI_R_N	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	50
	2TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	2TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE 1TO1 45S	*	1TO1 DIFFPAIR	=45 OHM SE	=45 OHM SE	=45 OHM SE	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
SENSE 1TO1 P2MM	*	1TO1 DIFFPAIR	0 200 MM	0 100 MM	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
THERM 1TO1 45S	*	1TO1 DIFFPAIR	=45 OHM SE	=45 OHM SE	=45 OHM SE	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
SPKR DIFFPAIR	*	1TO1 DIFFPAIR	0 300 MM	0 100 MM	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2 1 SPACING	?
THERM	*	=2 1 SPACING	?
AUDIO	*	=2 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND P2MM	*	0 20 MM	10000
PWR P2MM	*	0 20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	GND	*	GND P2MM
CPU VCCSENSE	GND	*	GND P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK PCIE	*	GND P2MM
GND	PCIE*	*	GND P2MM
GND	SATA*	*	GND P2MM
GND	USB*	*	GND P2MM
GND	LVDS*	*	GND P2MM
SB POWER	CLK PCIE	*	PWR P2MM
SB POWER	SATA*	*	PWR P2MM
SB POWER	SATA*	*	PWR P2MM

J11/J13 Specific Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	INLET_THMSNS_D1_P	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	INLET_THMSNS_D1_N	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBTTHMSNS_D2_R_P	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBTTHMSNS_D2_R_N	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBTTHMSNS_D2_P	
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBTTHMSNS_D2_N	
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBT_MLBBOT_THMSNS_P	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	TBT_MLBBOT_THMSNS_N	44
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE DIFFPAIR	THERM 1TO1 45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	TBDTHMSNS_D2_P	44
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	TBDTHMSNS_D2_N	44
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	CPUTHMSNS_D2_P	44
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	CPUTHMSNS_D2_N	44
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	CPUVR_ISNS1_P	42 52
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	CPUVR_ISNS1_N	42 52
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	CPUVR_ISNS2_P	42 52
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	CPUVR_ISNS2_N	42 52
	SENSE 1TO1 P2MM	SENSE	CPUVR_ISNS1_P_R	42 43
	SENSE 1TO1 P2MM	SENSE	CPUVR_ISNS1_N_R	42 43
	SENSE 1TO1 45S	SENSE	CPUVR_ISUM_R_P	42
	SENSE 1TO1 45S	SENSE	CPUVR_ISUM_R_N	42
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	ISNS_CPUDDR_P	42
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	ISNS_CPUDDR_N	42
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_P3V3S5_N	42
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_P3V3S5_P	42
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_3V3_S0_P	
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_3V3_S0_N	
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_CAMERA_P	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_CAMERA_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_P3V3_S0_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_P3V3_S0_P	41
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	ISNS_1V05_S0_P	42 55
SENSE DIFFPAIR	SENSE 1TO1 P2MM	SENSE	ISNS_1V05_S0_N	42 55
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_BMON_GAIN_P	
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_BMON_GAIN_N	
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_COMPUTING_N	41 43
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_COMPUTING_P	41 43
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_OTHER_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_OTHER_P	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_1V2_S3_N	41 53
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_1V2_S3_P	41 53
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_AIRPORT_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_AIRPORT_P	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_SSD_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_SSD_P	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_LCDBKLT_N	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_LCDBKLT_P	41
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_PANEL_N	43
SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_PANEL_P	43
DIFF SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_GAIN_N	43 44
DIFF SENSE DIFFPAIR	SENSE 1TO1 45S	SENSE	ISNS_HS_GAIN_P	43 44
AUD DIFF	1TO1 DIFFPAIR	AUDIO	SPKRAMP_INR_P	47 61 65
AUD DIFF	1TO1 DIFFPAIR	AUDIO	SPKRAMP_INR_N	47 61 65
	1TO1 DIFFPAIR	AUDIO	MAX98300_R_P	47
	1TO1 DIFFPAIR	AUDIO	MAX98300_R_N	47
SPKR OUT	SPKR DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	47 64
SPKR OUT	SPKR DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	47 64
		SB POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 62 64 65
		SB POWER	PP3V3_S0	8 11 12 13 15 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61
	GND		GND	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD 45SE	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE		

SD Card Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SDDATA	SD_45SE		SDCONN_DATA<0..3>	33 34
SDCLK	SD_45SE		SDCONN_CLK	33 34
	SD_45SE		SDCONN_WP	33 34
	SD_45SE		SDCONN_CMD	33 34
	SD_45SE		SDCONN_DETECT_L	33 34
	SD_45SE	SPI	SD_SPI_CLK	34
	SD_45SE	SPI	SD_SPI_CS_L	34
	SD_45SE	SPI	SD_SPI_MOSI	34
	SD_45SE	SPI	SD_SPI_MISO	34
	CLK_25M_45S		SDSCLK_CLK_25M_X1	
	CLK_25M_45S		SDCLK_CLK25M_X2_R	34 69

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